Full-wave Characterisation of RF Ceramic Packages

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***Abstract* — The characterization of small complex ceramic packages with (monolithically) integrated microwave circuits is investigated using full-wave methods. In order to correctly design packaged radio frequency (RF) chips, the consideration of the package has become an indispendible part of the chip design process, as the electrical properties of the package have a great impact on the performance of the RF chips. For an effective simulation, a segmentation between the chip and its immediate environment, such as, the package, is investigated, and a suitable interface between chip and package is proposed to prove the validity of the interface, the simulation of the packaged RF device, which is pieced together from the full-wave simulation of the package and the simulation of the RF chip, is compared to the corresponding measurement. Simulation and measurement of the packaged RF device agree very well.**

I. Introduction

The commercial success of mobile communication systems is accompanied by an increasing pressure to reduce price, size, and weight. Maintaining or even increasing technical performance and reliability, all components and their packages have to be reduced in size, and the complete RF front-end has to be integrated in a much smaller volume. This automatically leads to more complex packages and to increased integration density.

Another development is the trend towards complex modules, e.g., a complete RF section of a mobile phone [1], which is mounted on a multilayer printed circuit board (PCB) with a standard SMT solder process. Packaged chips and modules in the mm-wave frequency range are investigated in [2].

At these frequencies, a good interconnect technique for low return and insertion loss is required[3]. At low frequencies, however, combined with high integration density, interaction and interference between the different structures of a circuit play an increasing role. For example, output to input isolation is vital for amplifiers or filters to prevent unwanted feedback or filter stopband deterioration, respectively. The full-wave calculation of a simpler package is described in [4], and some slightly more complex arrangements are investigated with approximate techniques in [5]. The latter methods use lumped element approaches and do not consider electromagnetic effects exactly enough.

This article presents a full-wave characterisation of complex packages. Discrete ports are used in the interior of the package, thus the simulation results can be used with different chips. This segmentation of package (together with the PCB) and chip is validated experimentally. A method to analyze and compensate parasitic reactances introduced by the numerical implementation of these discrete ports will be shown, and recent simulation results of both a planar inductor and a ladder-type reactance filter in a package are presented.

II. Validation of the Modular Concept

A major goal of this work was to provide an accurate and effective simulation of packaged microwave chips, maintaining a maximum of flexibility to use the simulations for different types of chips or even different ways to characterize the chip itself. To this end, the whole structure is segmented into two sections (Fig. 1). The first section comprises the chip (e.g. MMIC or passive filter chip) and the bonding wires. The second section consists primarily of the package causing many effects and secondly of the measurement test fixture.

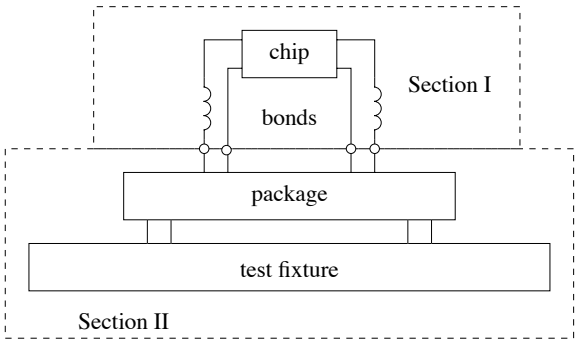

Fig. 1. Block diagram of the package structure

A. Validation of the Segmentation using Measurements

To ensure the validity of the segmentation, a number of test circuits are designed, fabricated, and measured. For the tests, the chips are die bonded into a $3\,\mathrm{mm} \times 3\,\mathrm{mm}$ ceramic package SMP-12 and electrical connection is achieved using wire bonding. As test chip a single acoustic resonator is used. A great advantage of such a resonator for the test is the fact that its reflection coefficient covers a large area of the smith chart. In a first step, the scattering parameters of the chip, the package, and the combination of both are measured with an on-wafer-prober. Following this, the scattering parameters of the complete arrangement are calculated from the separate

measurements of chip and package and compared with the overall measurement. The results are presented in Fig. 2 showing an excellent agreement of both curves, although the electromagnetic coupling between the chip and the package is neglected using this segmentation technique.

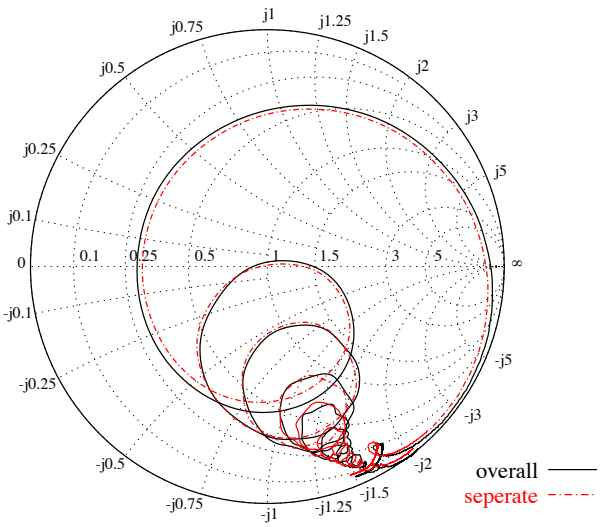

Fig. 2. Comparison of the return loss originating from the overall measurement of the packaged acoustic resonator and the cascaded individual measurements of the package and the acoustic resonator.

B. Segmentation within Full-Wave Simulations

As mentioned above, the segmentation of the packaged circuit is not only used to realise a modular simulation and design process, but also to combine the results from different simulation approaches.

Usually, scattering parameters are calculated based on transmission lines or “waveguide” ports. Such ports are defined in a cross section of the respective transmission line (reference plane). Many commercial 3D full-wave simulators exhibit an additonal limitation that these waveguide ports have to be located on the border of the simulation area. One example of calculating a packaged chip, using only waveguide ports, is presented in [6]. The segmentation into two sections is performed on-chip. In this case, the inner ports are realized as on-chip microstrip waveguide ports. This procedure unfortunately is not compatible with the modular concept as intended here, because parts of the chip already belongs to the package section.

An alternative approach is the usage of discrete ports or inner ports[4]. Such ports no longer require the existence of physical transmission lines as they are defined between two nodes. Circuit simulators based on lumped elements typically use these ports. Therefore, results from full-wave simulations with discrete ports can be easily combined with results from circuit simulators. One problem with the use of discrete ports in full-wave simulators, however, is the existence of parasitic effects introduced by the numerical implementation.

III. Parasitic Effects due to Discrete Ports

In space-discretized time-domain simulations (e.g. FDTD), bond contacts and ground pads, forming the physical nodes of an internal port in a package, are separated by a number of discretization cells. In the numerical procedure, however, an internal port is defined solely as a gap along the edge of a single cell. To provide a connection between the physical nodes and the ”numerical” port, the electric field at the connecting edges of the mesh between physical and numerical node are set to zero, thus forming an ideal, infinitely thin conductor along the connection path. This conductor is associated with a parasitic inductance. In reality, this inductance does not exist, as physically, the interconnections are made between bond pads and not between the virtual nodes in the discretization mesh. In addition, a parasitic capacitance is formed by the two parallel cell walls at the virtual gap port[7]. The parasitic effects of discrete ports are equal to those which occur when lumped elements, e.g. discrete resistors or diodes, are included in the FDTD mesh. One solution to overcome this problem is presented in [8]. In this approach an interface between FDTD and lumped elements is developed to include the lumped elements directly in the FDTD simulation, such that only one simulation is necessary to predict the overall performance of the circuit. In this way, the appearance of non-physical parasitic effects is suppressed. The procedure selected in this work does not suppress the appearance, bot allows to calculate and to compensate the parasitic effects in a second step.

The parasitic cell capacitance at the gap port is calculated as:

$$C_z = \varepsilon \frac{\Delta x \Delta y}{\Delta z}$$

Here the port is assumed to have an orientation in z-direction. In order to calculate the inductance, the radius of the wires has to be known. From this, the calculation of the inductance is straightforward.

A. Effective Radius of a Perfectly Conducting Cell Edge

In the area immediate around the wire, the circumferential magnetic field components and the radial electric field components can be assumed to vary as $1/r$ [9], where r is the distance from the wire. Using this assumption, the field components as shown in Fig. 3 can be described by

$$H_y(x) = H_y|_{i+1/2,j,k+1/2} \cdot \frac{\Delta x}{2(x - i\Delta x)}\,, \tag{1}$$

$$E_x(x, k\Delta z) = \begin{cases} 0 & \text{for } x - i\Delta x < r_{\text{eff}} \\ E_x|_{i+1/2,j,k} \cdot \frac{\Delta x}{2(x-i\Delta x)} & \text{for } x - i\Delta x \geq r_{\text{eff}} \end{cases}, \tag{2}$$

$$E_z(x) = \begin{cases} 0 & \text{for } x = i\Delta x \\ E_z|_{i+1,j,k+1/2} & \text{for } x = (i+1)\Delta x \end{cases}. \tag{3}$$

Applying Faraday’s law along contour k (Fig. 3), and considering (1)–(3), the time derivative of the magnetic

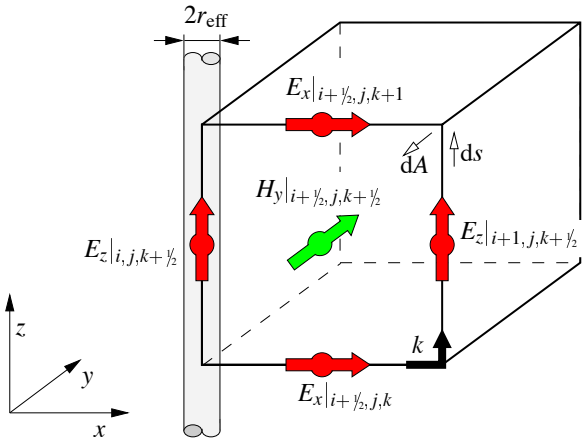

Fig. 3. Thin wire along a cell edge; Faraday's law contour path.

field component can be written as:

$$\frac{H_y|^{n+\frac{1}{2}}_{i+\frac{1}{2},j,k+\frac{1}{2}} - H_y|^{n-\frac{1}{2}}_{i+\frac{1}{2},j,k+\frac{1}{2}}}{\Delta t} = \frac{1}{\mu}\left(\frac{2}{\ln\frac{\Delta x}{r_{\text{eff}}}}\frac{E_z|^n_{i+1,j,k+\frac{1}{2}}}{\Delta x} - \frac{E_x|^n_{i+\frac{1}{2},j,k+1} - E_x|^n_{i+\frac{1}{2},j,k}}{\Delta z}\right). \tag{4}$$

The same component written in terms of the ordinary Yee algorithm[10] yields

$$\frac{H_y|^{n+\frac{1}{2}}_{i+\frac{1}{2},j,k+\frac{1}{2}} - H_y|^{n-\frac{1}{2}}_{i+\frac{1}{2},j,k+\frac{1}{2}}}{\Delta t} = \frac{1}{\mu}\left(\frac{E_z|^n_{i+1,j,k+\frac{1}{2}}}{\Delta x} - \frac{E_x|^n_{i+\frac{1}{2},j,k+1} - E_x|^n_{i+\frac{1}{2},j,k}}{\Delta z}\right). \tag{5}$$

Comparing (4) and (5), the effective radius of the perfectly conducting cell edge can be determined:

$$\frac{2}{\ln\frac{\Delta x}{r_{\text{eff}}}} = 1 \quad \Rightarrow \quad r_{\text{eff}} = \frac{\Delta x}{\mathrm{e}^2}.$$

Accordingly, a perfectly conducting cell edge acts like a thin wire with radius r_{eff}.

B. Inductance of a Perfectly Conducting Thin Wire

In a first step, a wire with homogeneous current density over cross section A is considered. Dividing the cross section in infinitesimally small current filaments, the inductance L of the wire is given by

$$L = \frac{1}{A^2}\iint_A\iint_A \mathrm{d}M\,\mathrm{d}A\,\mathrm{d}A. \tag{6}$$

According to [11], the mutual inductance of two current filaments with lengths l and distance r can be approximated by

$$\mathrm{d}M = \frac{\mu_0}{2\pi}l\left(\ln\frac{2l}{r} - 1\right) \quad \text{for} \quad \frac{r}{l} < 0.1.$$

Solving (6), the inductance of a wire with rectangular cross section $a \times b$ results in

$$L = \frac{\mu_0}{2\pi}l\left(\ln\frac{4l}{a+b} - \frac{1}{3}\ln 2 - \frac{\pi}{3} + \frac{13}{12}\right). \tag{7}$$

Eq. (7) includes the approximation that a square wire, with the same circumference as the rectangular wire, has the same inductance.

In the case of a perfectly conducting wire at microwave frequencies, the current flows only at the surface of the wire. To obtain the correct inductance, the inner inductance has to be subtracted from (7). The inner inductance of a rectangular wire with homogeneous current density[7] can be expressed as

$$L_{\text{i}} = \frac{\mu_0}{24}l.$$

For a connecting wire, spanning n cells in z-direction in the FDTD mesh, the final inductance is obtained as

$$L = \frac{\mu_0}{2\pi}n\Delta z\left(\ln\frac{2n\Delta z}{\Delta x + \Delta y} - \frac{1}{3}\ln 2 - \frac{5\pi}{12} + \frac{37}{12}\right).$$

Both the cell capacitance and the connecting wire inductance depend on the mesh discretization. The parasitic effects can be eliminated in a post-processing step by using a suitable compensation network composed of lumped elements.

IV. Comparison to Measurement

A. Planar Inductor

As a first example, a planar inductor is chosen to validate the segmentation into two sections using full-wave simulations. One advantage of this example is the possibility to simulate also the whole structure (planar inductor in the package) as a whole, too. The inductor is fabricated on a commonly used RF substrate, glued into the package and connected using wire-bonding. The package is soldered onto a test board, with two SMA-connectors. The measurements are performed with a network analyser, calibrated on coax level. In parallel, the complete arrangement is modeled in the field-simulator. In Fig. 4 the insertion loss of the packaged planar inductor is shown. Both simulations – those of the separate parts connected via discrete ports as well as the simulation of the complete structure – match the measurement very well.

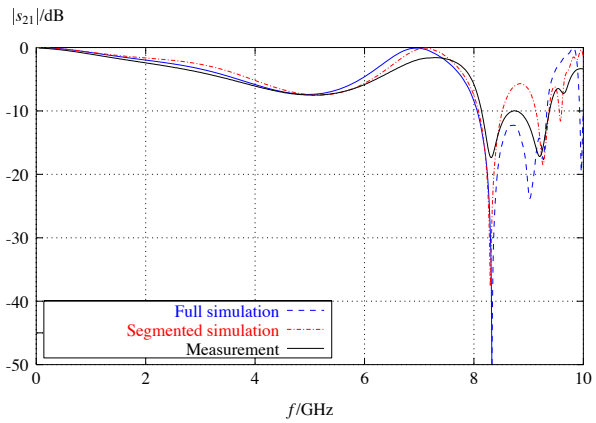

Fig. 4. Insertion loss of the packaged planar inductor. Comparison of the segmented structure with those of a full simulation and those obtained by measurement

B. Ladder-Type Reactance Filter

As a second example, a ladder-type reactance filter with a center frequency of 1.84 GHz is investigated. In these filters, the reactances of acoustic resonators are used to shape the desired filter characteristic. Therefore, parasitic reactances have a great impact on the filter performance. Furthermore, the filter, used as example, has a high center frequency, so the electromagnetic effects in the package are more pronounced. To predict the overall filter performance of the packaged filter, a very accurate package simulation is necessary. Two waveguide ports and six compensated discrete ports are used to simulate the package. A full-wave simulation of the filter chip itself is not reasonable, because the structures on the filter chip are very small ($< 1\,\mu$m), so that simulation time and memory requirement are beyond present possibilities. Another problem is the piezoelectric effect, which is not included in many of today's field simulators. Consequently, to simulate the filter chip itself, other methods are used [12]. The scattering parameters of the two independent simulations then are cascaded in the frequency domain. Fig. 5 shows the comparison of the measurement and the result of the simulation, providing a very good agreement over a wide frequency range. Also the return loss in the passband of the filter is excellently predicted, as shown in Fig. 6.

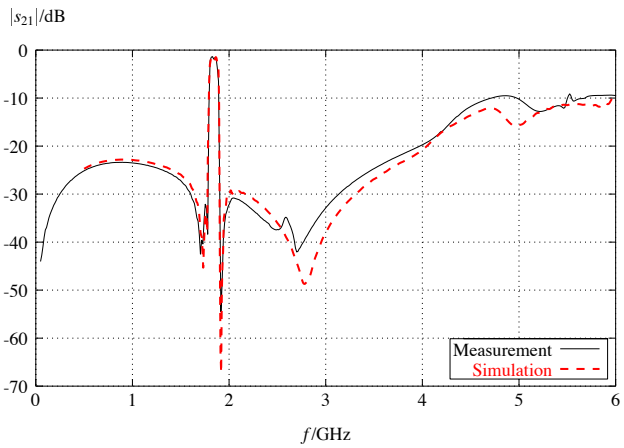

Fig. 5. Comparison of theoretical and experimental insertion loss of a packaged filter over a broad frequency range

V. Conclusions

In this paper, a full-wave characterization of a ceramic package is presented. The main goal was to obtain an accurate package description, which can be used with different chips placed into the package. The excellent prediction of the overall performance applying the segmentation approach as described in this paper enables the reduction of prototype cycles designing new packages or chips. The accurate package characterization is gaining increased importance, if several chips are integrated in a single package (MCM Multi-Chip-Module) or if passive components are integrated in the package.

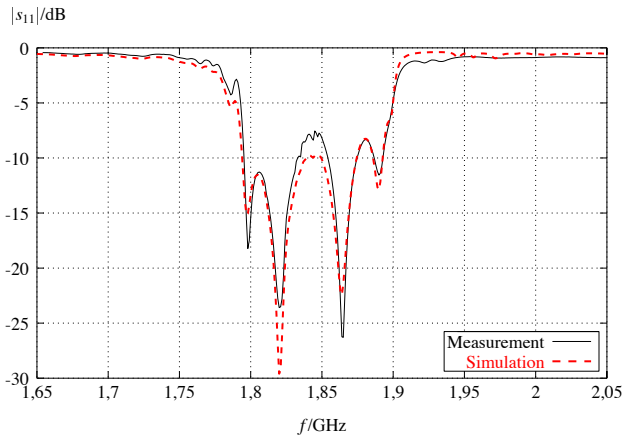

Fig. 6. Comparison of theoretical and experimental return loss of a packaged filter

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