RF and SAW Package Simulation

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ABSTRACT — **An accurate electromagnetic characterization of packaged integrated circuits mounted on a carrier substrate is presented in this contribution. Both the base substrate of the package and the carrier substrate may be complex multilayer arrangements. As a MMIC or a SAW filter - at least with present state-of-the-art simulators - can not be included into a complete overall electromagnetic simulation, only carrier substrate and package are simulated as a whole, and the chip performance (calculated by other methods or characterized by measurements) is included using network techniques. For interconnects within the package, special care has to be taken to include all parasitics, e.g. of bond wires and of effects possibly introduced by the simulation tool.**

Both in a test as well as in an application environment, the layer structure and metallization pattern of the carrier substrate have to be selected carefully to prevent coupling between input and output or unwanted resonances. As a result of all these efforts, an accurate prediction of the performance of packaged devices on multilayer substrates is possible.

I. INTRODUCTION

The last years have seen a dramatic increase of RF and microwave applications both for commercial and consumer application, including mobile phones, bluetooth, WLAN, or automotive applications. Frequencies range from hundreds of MHz to 77 GHz for automotive radars. This trend would not have been possible without tremendous progress in RFICs or MMICs, CAD systems, integration and packaging techniques, and fabrication methods suitable for low-cost mass production. In parallel, integration density has been increased continuously, and in spite of more and more complex systems, development cycle time and cost have been reduced, too.

Earlier solutions for RF and microwave systems were based on "chip and wire", mostly realized as individual solutions (special substrates, custom designed housings, specialized machines…). Parallel to this, the high pin count of signal processing circuits led to the development of new substrate techniques (e.g. ceramic multilayer), surface mounting of devices and ICs, flip-chip, or ball grid arrays. In the last years, these techniques have been refined continuously and have become more accurate. Consequently, they have found increasing interest and have been introduced to RF, microwave, and even mm-wave systems, e.g. [1 – 4].

For such applications, the types of substrates are selected according to the high frequency requirements, available production facilities, and minimum cost. This may often lead to a mixture of substrates e.g. "standard" multilayer printed circuit boards (PCBs) for power supply, signal processing circuits, IF and baseband circuitry, or even simple high frequency interconnect lines [3]. Improved requirements can be met using LTCC (or HTCC for high power), e.g. for passive devices. If necessary, small pieces of special microwave substrates may be used for critical functions like microwave filters [5]. Discrete semiconductor devices, MMICs, or SAW chips connected to the passive circuits typically require some protection against environmental influences like moisture. Some recent efforts use plastic underfill or glob-top approaches (shielding devices or chips with some drop of plastic) [4]. For SAW chips and a number of MMICs, however, any material placed directly on top of the circuit would completely destroy or deteriorate its function. Therefore, special (hermetic) packages are necessary.

A package itself often consists of a multilayer ceramic substrate, possibly with a cutout for the chip, bonding pads insides, and contact pads at the outside. The chip is glued or soldered into the package and connected to the respective interconnect pads. The package then is closed using a (metal) cap. The packaged device finally is placed onto the carrier substrate, either in a test or in the

application environment, and connected to the surrounding circuitry (Fig. 1). The associated problems will be pointed out in the following.

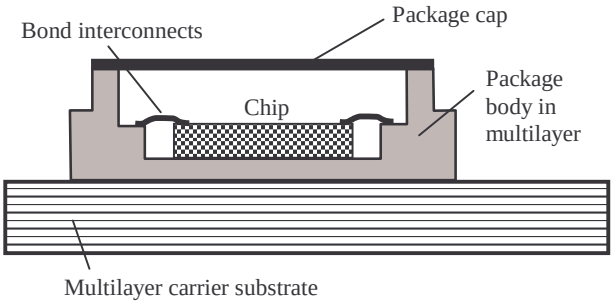

Fig. 1: Principle configuration of a packaged chip on a multilayer carrier substrate.

- Both MMICs and SAW circuits typically are too complex to allow a full-wave simulation (including a combined surface acoustic wave/electromagnetic simulation in the SAW device case). Circuit performance therefore is available on the basis of approximate (electromagnetic) calculations, circuit based simulations, or measurements only.
- In a number of cases, there are no interfaces or reference planes with defined transmission line structures and transmission line modes at the interconnects between chip and package. In some cases, the same is true for the interfaces between package and carrier substrate.
- Chip, package, and the circuit structure of the carrier substrate around the package may form a rather complex three-dimensional electromagnetic configuration.
- Dimensions occurring in the assembly of chip, package, and carrier substrate vary from micrometer to millimeter. This proves extremely challenging for an electromagnetic (EM) simulation of the overall arrangement or even parts of it.
- The packaged chip will be employed in different environments (different applications, different system manufacturers). The supplier of the packaged chip, however, should test and document the performance of the device as general as possible, i.e. if ever possible, independent of the application environment, or a preferred device environment compatible, however, with the application environment should be specified.
- Carrier substrate and package of the device should have none or hardly any effect on the device performance. With increasing miniaturization, however, this gets more and more difficult. Amplifiers may suffer from unwanted feedback, or highly selective filters may show a reduced isolation due to signals leaking directly through the package or carrier substrate.

II. Some General Considerations for the Circuit Simulation

A. Simulation Tools

At least at lower frequencies, e.g. for mobile phones (roughly 300 mm or 150 mm wavelength), many circuits seem to be small compared to wavelength; so the possibility of quasi-static methods based on the calculation of capacitances and inductances [6] often is considered sufficient. This, however, is not always true as will be demonstrated at an example of a packaged SAW filter on a PCB carrier substrate. Fig. 2 shows its insertion loss results computed with both a quasi-static method and a full-wave method as described later on, together with experimental results. While the performance in the passband is simulated sufficiently well with both methods, an increasing discrepancy occurs in the stopbands below and above the passband. Apparently, effects like a high dielectric constant, increased internal line lengths, or more complex coupling due to the complicated structures play an increasing role for such circuits. This clearly demonstrates the necessity for improved simulation tools to better predict the circuit performance in the critical rejection bands and to allow less experimental optimization iterations and shorter overall design cycles.

For purely planar circuits (with the dielectric substrates extending to infinity), method of moment (MoM) tools are ideal, as they reduce the three dimensional problem to a two-dimensional one, i.e. the computation of the current density in the planar conductors. In the case of three-dimensional metallization structures like vertical interconnects, vias, or bond interconnects, or with dielectric substrates of finite size, however, these tools loose their main advantage and get computationally more expensive. In addition to numerous in-house solutions, a number of commercial simulators on this basis are readily available, e.g. [7, 8].

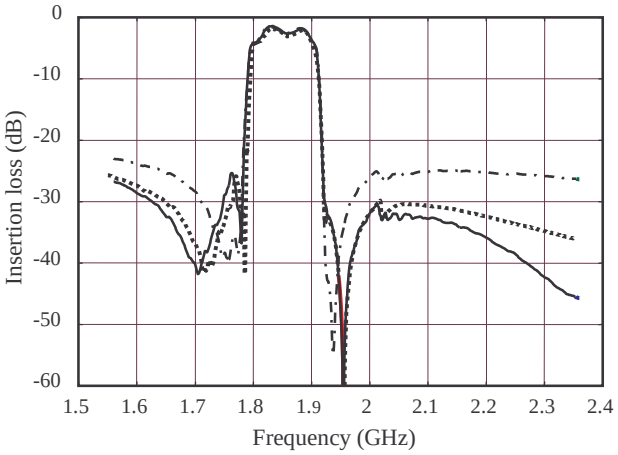

Fig. 2: Insertion loss of a packaged SAW filter on a PCB carrier substrate. Solid line: experiment, dash-dotted line: quasi-static simulation, dotted line: full-wave simulation.

In the last decade, electromagnetic field simulators based on finite element (FE), finite difference (FD), or finite integration (FI) methods have provided flexible tools to analyze nearly arbitrary three-dimensional structures, e.g. [9 - 11], often as time domain (TD) simulators. Although such methods require a lot of memory and computation time, various improvements have made these tools more practical and indispensable for the design of complex three-dimensional circuits

B. Segmentation of circuits

Typically, the necessary computational effort increases over-proportionally with the number of cells in which the circuit has to be divided for simulation. Therefore, attempts are made to divide the circuits into smaller units which are computed separately. The overall performance then is calculated by network methods. This procedure, however, requires defined interfaces between the different parts, typically reference planes on a transmission line with discrete modes, but also more general waveguide type cross sections can be used [12]. Such a procedure, however, fails in the case of complex electromagnetic field interactions.

In the arrangements considered in this contribution, there is a multilayer PCB, a package, and a chip with an integrated circuit in the package. In principle, all three parts could be analyzed separately as *n*-ports (as has been done, for example, for a package in [13]) and connected at the respective ports. In some cases, however, combining two parts may change the EM environment of one or both parts. For example, a metal package influences the EM field distribution on top of a carrier substrate, leading to wrong results for the combination of the separate calculations.

As already mentioned above, however, a MMIC or a SAW circuit mostly are not accessible to a full-wave simulation, and consequently, no full-wave simulation of the overall combination of substrate, package, and chip is possible. Fortunately, the integrated circuits often are placed on a ground metallization within the package, thus segmentation at this position seems to be possible. To test this, a single SAW resonator was first measured separately placed on a special metal carrier and using on-wafer probing. The input reflection coefficient of the resonator covers a very wide range of values; therefore, this was regarded as an ideal test structure. Parallel to the resonator, the combination of substrate and package was measured as a four-port (once again in a special test arrangement). Finally the overall circuit with the resonator placed into the package was measured, too. The overall measurements then were compared with the s-parameters calculated from the measurements of the separate parts (including an inductance and a resistor for each bond interconnect).

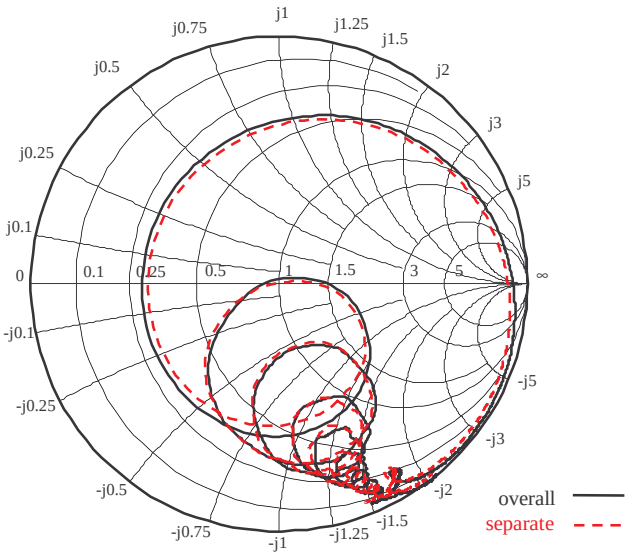

Fig. 3: Input reflection coefficient of a packaged SAW resonator. Solid line: overall measurement; dashed line: measurements of PCB/package and SAW resonator as single structures, the combined performance is calculated from these separate measurements.

Fig. 3 shows a Smith chart plot of the input reflection coefficient S_{11} of the resonator. An excellent agreement can be stated over the complete frequency range (up to 1.1 GHz shown here, but the same is true up to 5 GHz),

especially considering that S_{11} passes through nearly the complete chart [14]. In addition, a number of full-wave simulations were done proving that this approach is acceptable.

The segmentation of substrate/package and chip is demonstrated here at the example of a SAW circuit, but it should work equally for a MMIC based on microstrip technology with ground plane under the chip.

C. Port selection/implementation of "lumped" circuits

In this work, carrier PCB and package are handled and simulated as a single unit. The outside ports do not provide any problem; they are either standard planar transmission line ports, or even the transition to coaxial connectors may be included into the simulation [15]. This is completely different for the inside ports of the package. Typically, there are simple bond pads, and the MMIC or the SAW filter is connected using bond wires or ribbons. (For higher frequency or mm-wave MMICs, however, efforts are made to provide a transmission line interface in the package interior, too, as standard loop-type bond interconnects provide unacceptable parasitics). Fortunately, most simulation tools include so-called discrete ports based on voltage and current.

In space-discretized time-domain simulators (e.g. FDTD), bond contacts and ground pads, forming the physical nodes of an internal port in a package, are separated by a number of discretization cells. In the numerical procedure, however, an internal port is defined solely as a gap along the edge of a single cell. To provide a connection between the physical nodes and the ”numerical” port, the electric field at the connecting edges of the mesh between physical and numerical node are set to zero, thus forming an ideal, infinitely thin conductor along the connection path. This conductor is associated with a parasitic inductance [16, 17]. In reality, this inductance does not exist, as physically, the interconnections are made between bond pads and not between the virtual nodes in the discretization mesh. In addition to the inductance, a parasitic capacitance is formed by the two parallel cell walls at the virtual port gap [16]. The parasitic effects of discrete ports are equal to those which occur when lumped elements, e.g. discrete resistors or diodes, are included in the FDTD mesh. One solution to overcome this problem is presented in [17]. In this approach an interface between FDTD and lumped elements is developed to include the lumped elements directly in the FDTD simulation by spreading the lumped element across its complete volume, such that only one simulation is necessary to predict the overall performance of the circuit. In this way, the appearance of non-physical parasitic inductance and capacitance is suppressed. An alternate approach is not to suppress the appearance, but to calculate and compensate the parasitic effects in a second step. To this end, an effective radius of the mesh edges is computed [14]. From this, an equivalent inductance can be derived [14, 18] which finally is used (with negative sign) to compensate its influence at the respective interconnect. In a similar way, some lumped element can be connected between the edges of a single cell, and the missing influence of its physical size is accounted for by artificial parasitics subtracted from the lumped element values.

III. SUBSTRATE EFFECTS

While the desired signal path is from the PCB input via the package contacts to the chip and back out, there may be parasitic coupling through the PCB as well as through the package body (Fig. 4). This effect may lead to feedback and even oscillations in the case of a (high gain) MMIC amplifier or it may deteriorate the stopband performance of filters.

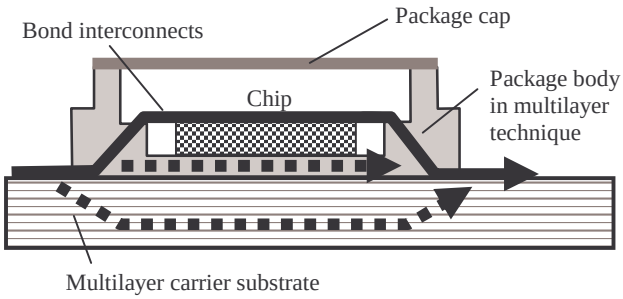

Fig. 4: Intended (solid arrow) and parasitic signal path (dotted arrows).

In the case of single layer substrates, such coupling often is caused by surface waves launched at discontinuities. In multilayer circuits, the most critical effects are due to unwanted modes, e.g. parallel plate modes between two different ground layers. Even if the two ground planes are connected by a number of vias, current through the vias may lead to some voltage drop. In signal processing circuits, this leads to the effect of "switching noise" [19]. At higher frequencies, resonances between rows of vias may occur. This is demonstrated at two examples. The first one concerns a test PCB with mixed microstrip/coplanar input and output lines. Top and lower ground planes are connected by double rows of vias (Fig. 5). The insertion loss of this test PCB without any package or device fixed on top is plotted in Fig. 6. A bandpass type characteristic slightly above 6 GHz can be observed. Looking in detail at the field distribution in the top dielectric layer, a half-

wavelength resonance is found, excited by the stray field of the connecting lines (and by the transitions to coaxial line). Of course, this resonance occurs as well with a (packaged) device mounted to the test PCB.

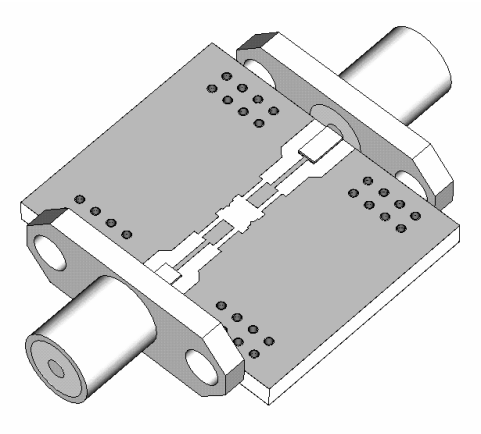

Fig. 5: Principle setup of a test PCB. The distance between the two double rows of vias is 20 mm.

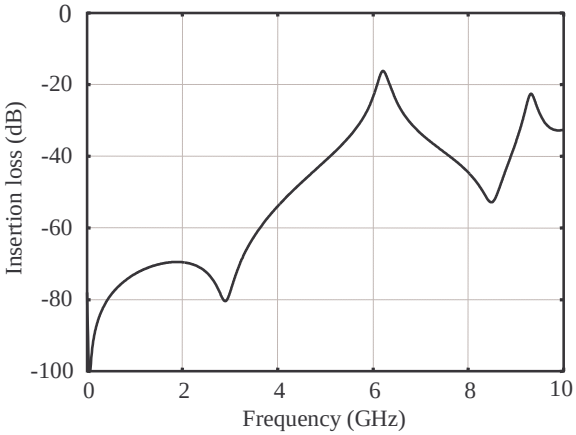

Fig. 6: Insertion loss of the empty test PCB according to Fig. 5.

The second example is a transition between a microstrip line on top of a multilayer LTCC substrate to a stripline in a lower substrate level as a potential feed-through into a package (Fig. 7). The two lines can either be connected by a via [20] or by EM field coupling through a slot in the upper ground plane [21]. In both cases, however, an asymmetry is introduced exciting a parallel plate mode between the two ground planes. Therefore, rows of vias have to be introduced to guarantee the desired field configuration (Fig. 8). Fig. 9 shows return and insertion loss calculated by an in-house FDTD code [17] for three different positions of the vias. In spite of a high number of vias, a resonance occurs in the frequency range between 30 GHz and 35 GHz. Care has to be taken to move the resonance out of the application band. Furthermore, this example demonstrates a possible problem using time domain codes. Typically, simulation is continued over a time as short as possible. Following this, the frequency response is calculated by a Fourier transform. If the number of time steps, however, is not large enough, the frequency resolution may not be fine enough to resolve the resonance. In this case, a system identification method [22] was used finally to get a better frequency resolution and to solve the problem.

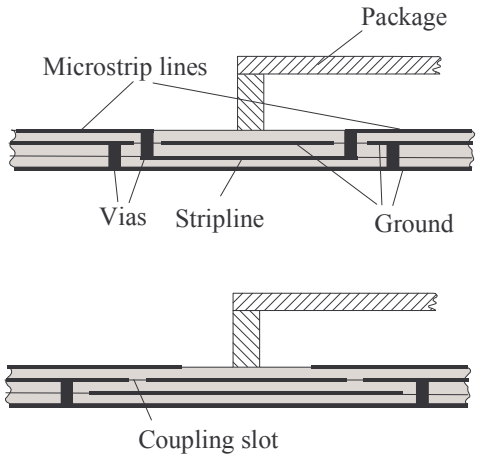

Fig. 7: Cross sections of two possible feed-through structures using multilayer substrates.

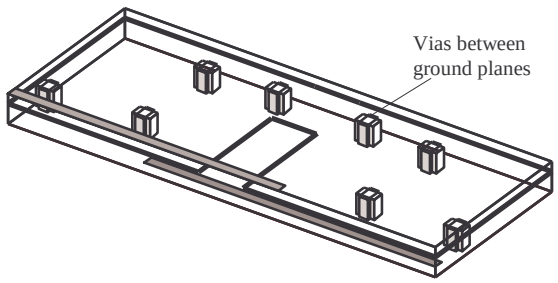

Fig. 8: Longitudinal cut through the transition according to Fig. 7 (bottom, with EM field coupling), showing the vias to suppress parallel plate modes.

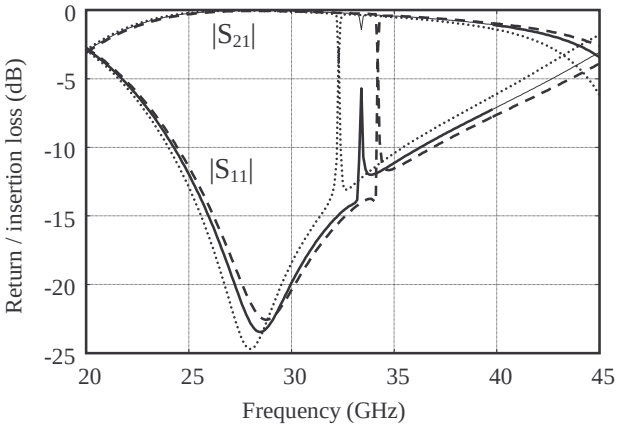

Fig. 9: Computed return and insertion loss of a slot-coupled transition according to Fig. 7 for different positions of the vias.

As indicated above with the first example, the choice of the PCB structure can influence considerably the overall circuit performance. The manufacturer of an integrated circuit has to provide and prove experimentally tight specifications for his device. Typically, however, test and application environment may differ considerably, e.g. in the metallization pattern of the chip landing area in a package or in the PCB layer dimensions. Fig. 10 gives the insertion loss of the same packaged SAW filter tested with two different PCBs.

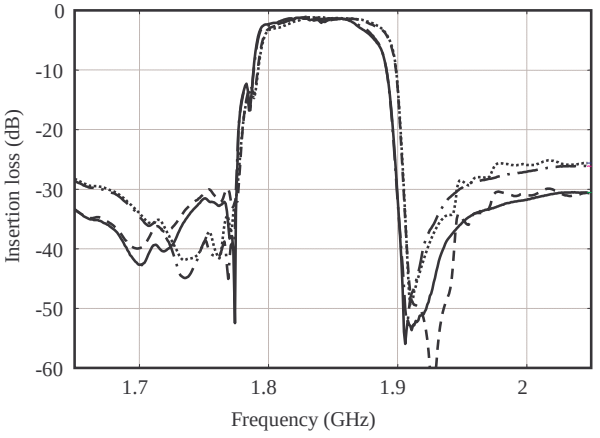

Fig. 10: Insertion loss of a packaged SAW filter placed on two different test PCBs. Solid line: theory for PCB 1; dashed line: experiment for PCB 1; dash-dotted line: theory for PCB 2, dotted line: experiment for PCB 2.

As can be clearly seen, strong differences occur in the lower and upper stopband, and even a slight change in center frequency, bandwidth, and passband ripple (not seen clearly in this figure) occur. On the other hand, the full-wave calculation as applied by the authors can predict these differences in an excellent way.

In practice, SAW filter performance must meet the specifications in different surroundings (different phone manufacturers, different types of phones, etc.). Consequently, a design and test environment as neutral as possible has to be used for testing, and possible recommendations for the immediate PCB environment may be given to the system manufacturers. Therefore, a number of measures were taken to improve the compatibility of test and application environment, even if the layer structures of test and application PCBs may be different. This includes [15]

- An improved transition from the coaxial test equipment to the planar lines on the PCB. In principle, these transitions can be characterized and the results de-embedded using a suitable calibration procedure, but this mostly is too time-consuming.
- Well defined planar lines (50 Ω impedance, single mode performance) on the PCB with minimum coupling between each other and remaining structures.
- A closed ground plane directly beneath the first dielectric layer. Thus, parasitic coupling to lower PCB levels is prevented.
- An optimized landing area (foot print) for the device with a sufficient number of vias to reduce inductance to ground and to decouple input and output.

An example of computed return and insertion loss of a SAW filter both in an optimized test as well as in a typical mobile phone environment is given in Fig. 11. Although the test PCB had a layer thickness of about 0.2 mm and the phone PCB of 0.06 mm only, an excellent agreement can be stated in these two environments.

IV. Final Example

All the techniques as described above finally were applied to the calculation of packaged chips on a PCB, including the full-wave calculation of the combination of PCB and package (and a separate description of the chip by other methods [23]), discrete ports inside the package with compensation of the parasitics, inclusion of bond inductance and resistance, and an optimized test environment. For comparison and demonstration of the different techniques, some results already have been included in Figs. 2, 10, and 11. To demonstrate that these techniques do not only succeed directly around the filter passband at relatively low frequencies, a final example is

presented in Fig. 12. The insertion loss is computed up to 6 GHz, and it still shows an excellent agreement with experiment (Fig. 12 a). In addition, also the passband return loss is predicted with good accuracy (Fig. 12 b).

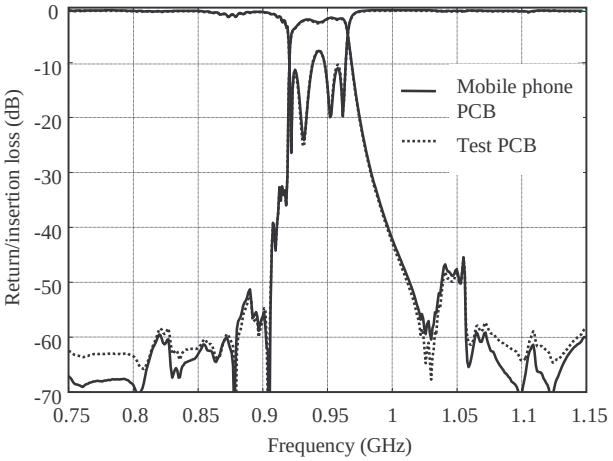

Fig. 11: Theoretical return and insertion loss of a SAW filter both on an optimized test PCB as well as on a typical phone PCB.

V. Conclusion

An accurate characterization of packaged chips on a multi-carrier substrate (PCB) has been demonstrated. A discrete time domain tool is used to compute PCB and package. Discrete ports, together with a compensation of their artificial parasitics, are used in the interior of the package. The chips are connected to these ports as separate, quasi-discrete devices. The chip performance, either of MMICs or SAW filters, can be characterized by different, problem-adapted methods or by measurements. A number of examples are given, showing an excellent agreement with experiment. Based on this, it is possible to predict the performance and to optimize both package and carrier substrate.

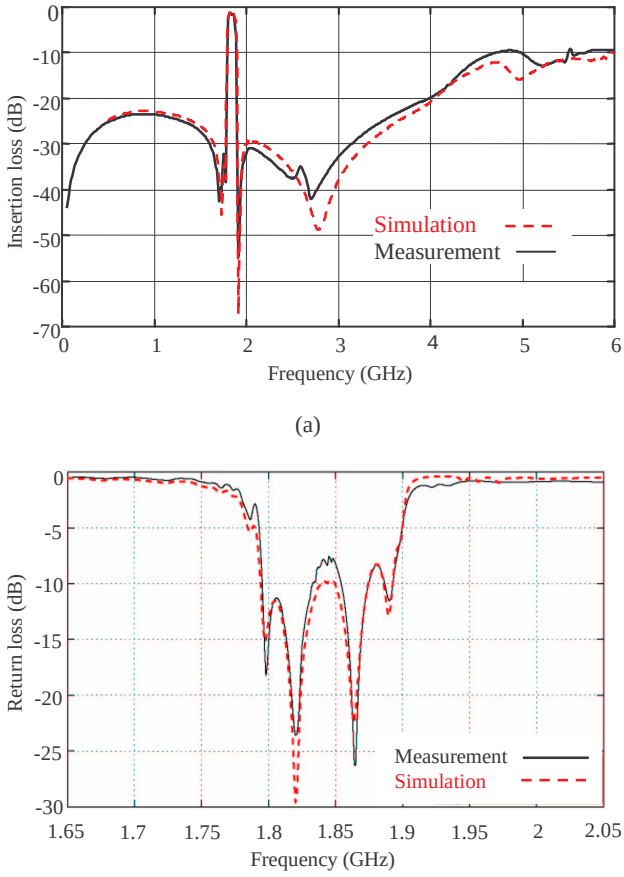

Fig. 12: Theoretical and experimental insertion (a) and return loss (b) of a packaged SAW filter on a test PCB.

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