A New Modular Design for Test and Application PCBs of SAW RF Filters to Ensure Precisely Predictable Filter Characteristics

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***Abstract*—The paper presents the design of an optimized test and application setup for SAW RF filters. These structures have been investigated, including the test-devices, by simulation techniques based on full-wave methods and common SAW simulation methods. In this contribution, the simulation technique will be explained in detail, focussing on the interfaces of the simulation models. Parasitic electromagnetic effects in the test and application setup will be analyzed by simulation and measurement. The paper demonstrates the possibility of accurate performance prediction of SAW RF filters using specially designed test setups in the measurement and an optimized application environment, e.g. in mobile phones. Modular parts for such test setups and the application environment are discussed.**

***Index Terms*— simulation methods, SAW, printed circuit board (PCB), measurement setup.**

I. Introduction

In the RF sections of mobile communication equipment, surface acoustic wave (SAW) radio frequency (RF) filters are key components. Within the past years, the size of the packages has been reduced from a typical form factor of 5.8 mm × 5.8 mm to 1.4 mm × 2.0 mm. Center frequencies have shifted from 1 GHz to above 2 GHz. At the same time, further functionality has been added to the pure filtering function [1]. Two examples of such additional functions are impedance transformation or balun functionality. Permanent quality enhancements in the field of wireless communication have forced manifold improvements of the filter performance regarding matching, close-in and far-off selectivity, and pass band attenuation.

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Furthermore, the design of SAW RF filters is an extremely time critical task, because the life cycle of mobile communication devices is relatively short. The design in a single iteration step is an important issue. Thus, the accurate prediction of the electrical characteristics of SAW RF filter by simulation and the verification of these by measurements has become a prerequisite for their efficient design [2]. Taking into account all relevant effects related to the package and the measurement environment in the simulation models is tedious. Up to now it is still a problem that the measurement environment, in particular the PCB on which the component is soldered for operation, can significantly influence the measured electrical characteristics [3] consequently. All its relevant effects and influences have to be implemented or sufficiently taken into account in the simulation for the filter design.

In [4] the differences in the electrical properties of test and application environment for SAW RF filters have been discussed, leading to a new design for the application environment. Thus, the performance of the filter in the application environment is precisely predictable by measurement results obtained with the test PCB.

This paper will give more detailed information concerning the simulation techniques used to optimize the described geometries. Furthermore a description of problems which appeared during the establishment of the simulation techniques is given. Appropriate solutions are described. Thus, parasitic effects inside a PCB, and the influence of these on the device under test (DUT) will be explained. Additionally all optimized geometries of test and application PCBs for SAW RF filters are shown in detail focussing on the discrepancy between measurement and application environment. The design of the geometries has been optimized towards minimal reflections, minimal feed-through or cross-talk, and minimal losses. Thus, the influence by the electrical characteristics of this PCB on the measured data of a SAW filter is drastically reduced. This is an important advancement in the design of test PCBs which are used to check the agreement of the performance of a SAW RF filter with its specifications.

Sec. II starts with an example comprising a couple of SAW filter setups that emphasizes the potential impact of PCBs on the electrical filter characteristics. Sec. III explains the

developed simulation techniques in two examples. Sec. IV shows strategies to avoid the parasitic effects in PCBs. These focus on the proposal of optimized modular parts for test PCBs. Additionally, Sec. IV explains a new application PCB with results being given in Sec. V. Sec. VI summarizes and concludes the paper.

II. Potential Parasitic Effects in the Package and the PCB

Fig. 1 shows the measurements of a SAW RF filter mounted on different test setups. These test setups comprise the PCB and the SMA-connectors used to connect the filter to the measurement equipment.

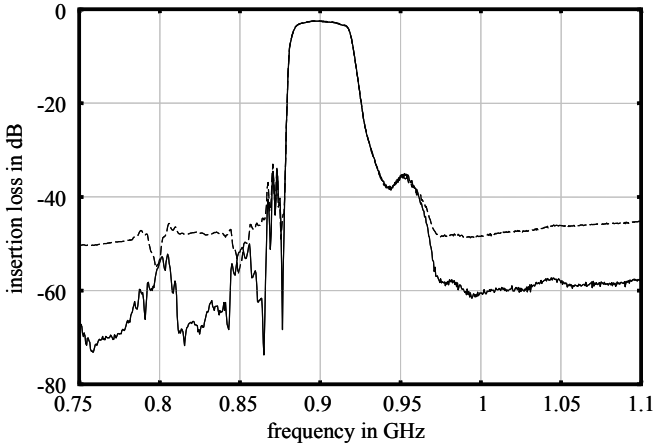

Fig. 1: Comparison of measured insertion loss of the same packaged filter assembled on two different PCBs.

As shown here, the attenuation in the lower and upper stop-band is significantly affected by the test-setup. According to these results, it can be assumed that there exists more than one signal path. These parasitic paths can be located in the PCB or in the package, and interaction between these paths is possible (Fig. 2).

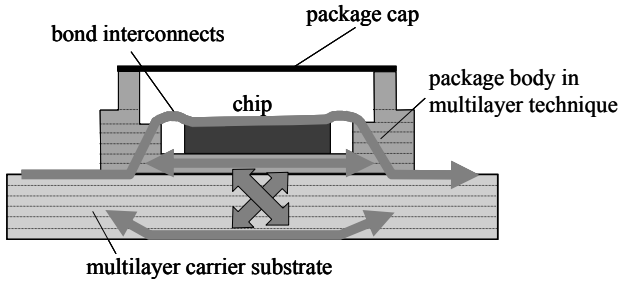

Fig. 2: Signal paths inside a setup of PCB, package and chip.

An accurate prediction of the whole setup is only possible with detailed information about the electromagnetic characteristics of its separate parts. For the test setup, for example, information about the transition from connectors to the soldering pad and about crosstalk is necessary. This topic is a serious task for application-near PCBs, as these are often based on very specific multilayer substrates. Fig. 3 shows the crosstalk inside such a multilayer PCB. The strong peaks in the crosstalk characteristic occur due to a resonance phenomenon.

This effect can be suppressed using vias for shielding purpose [5]. The second graph in the diagramm shows the results for a very similar PCB including such vias.

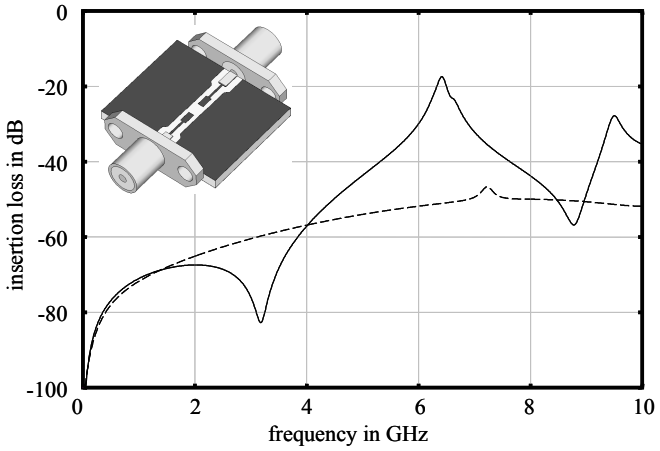

Fig. 3: Full-wave simulation results of two different test PCBs. One shows significant resonance phenomena (solid) at 6.5 and 9 GHz. The other is an improved version with suppressed PCB resonances (dashed).

Many circuits in mobile phones seem to be small compared to the wavelength (roughly 300 mm or 150 mm). So it may be assumed that quasi-static method can be used sufficiently for a simulation [6]. Fig. 4 shows exemplarily that this is not always true, giving the quasi-static and full-wave simulation results for the insertion loss of a packaged SAW filter in the measurement setup. While the performance in the passband is simulated sufficiently well with both methods, a significant discrepancy occurs in the stopbands below and above the passband.

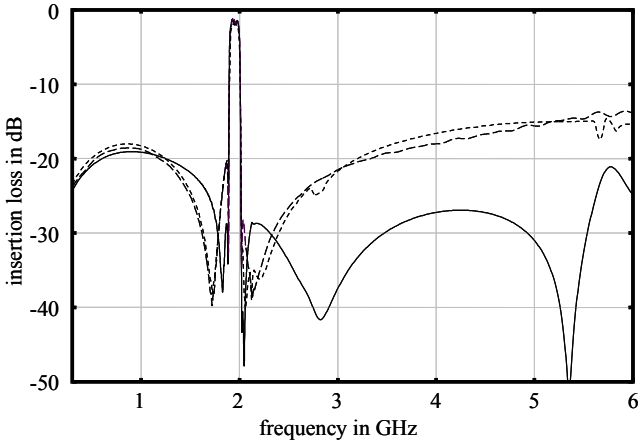

Fig. 4: Measured (dotted), full-wave-simulated (dashed) and quasi-static simulated (solid) insertion loss of a packaged SAW RF filter in the test environment.

Apparently, effects like a high dielectric constant, increased internal line lengths, or more complex coupling due to the complicated structures, which cannot be simulated sufficiently with quasi-static methods, play an increasing role for such circuits. This approach has been proven by another modified simulation of PCB and package, where the electromagnetic coupling beetween the feedthroughs of the package has been neglected. A comparison of the achieved results to the overall simulation is given in Fig. 5. This clearly demonstrates the

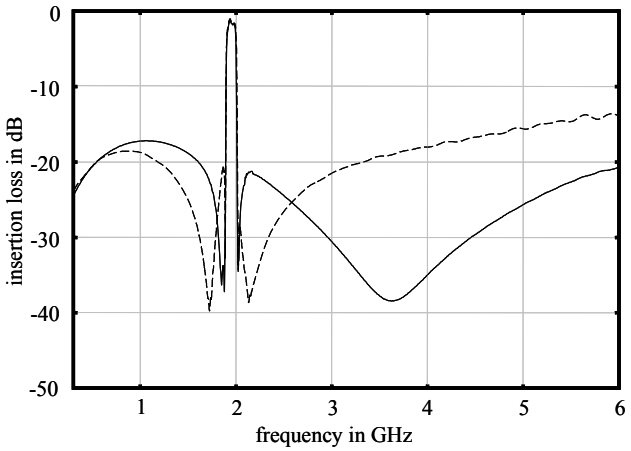

Fig. 5: Comparison of simulated insertion loss for an overall simulation (dashed) and a simulation with neglected electromagnetic coupling between feedthroughs of the package (solid).

necessity for improved simulation tools in order to predict the overall circuit performance accurately in the critical rejection bands, to reduce the number of experimental optimization iterations, and to allow shorter overall design cycles.

The excellent agreement between full-wave simulation and measurement results approves that all electrical properties of the simulated component have been taken into account sufficiently.

III. Simulation Techniques

A. Simulation Tools

For the configuration considered in this paper, two-and-a-half-dimensional solvers basing on the method of moments can only be used with constraints, as this method looses its main advantage and gets computationally very expensive for structures containing vertical interconnects, vias, or bond interconnects.

For the simulation of the discussed complex three-dimensional structures, 3D electromagnetic field simulators based on finite element (FE), finite difference (FD), or finite integration (FI) methods have provided flexible tools, often as time domain (TD) simulators.

Although such methods require a lot of memory and computation time, various improvements have made these tools more practical and indispensable for the design of complex three-dimensional circuits [7, 8].

For SAW chip simulation, techniques according to methods, explained in [9, 10], are used.

B. Segmentation of Circuits

For simulation methods using space-discretization, the computational effort increases over-proportionally with the number of mesh cells, into which the circuit has to be discretized for computation. Thus, the circuits are divided into the smallest subcircuits, which can be computed separately. The results for the subcircuits are then combined using network methods. Such a segmentation procedure, however, requires defined interfaces between the different functional parts, typically reference planes on a transmission line with discrete modes (more general: waveguide type cross sections). This technique cannot be used, if there exist complex electromagnetic field interactions in the separation area.

The setup which is simulated here consists of a multilayer PCB and a package with an integrated circuit in the package. Combining two parts may change the EM environment of one or both parts. For example, a metal package influences the EM field distribution on top of a carrier substrate, leading to wrong results for the combination of the separate calculations.

This phenomenon leads to even worse results when the interface to an MMIC or a SAW circuit has to be defined and consequently, no full-wave simulation of the overall combination of substrate, package, and chip is possible. Fortunately, the integrated circuit often has a metallized backside, connected to the ground structures of the package. Thus, port definition and segmentation seems to be possible. A number of full-wave simulations were done proving that this approach is acceptable.

As a test example, a planar microstrip inductor is used as test circuit. The measurement of the packaged inductor in a test setup is compared to the simulation results achieved by two different segmentations of the same model (Fig. 6). It is shown that the simulation result received from the segmentation, where package and test setup are included in one section, agree very well with the overall measurement. Large deviations appear, if an inappropriate model is selected.

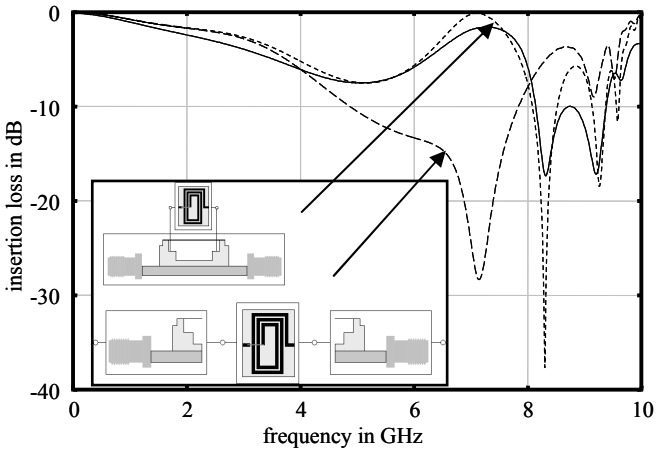

Fig. 6: Measured insertion loss (solid) of the whole setup and insertion loss from full-wave simulations of the differently segmented setup. The segmentations were implemented in an accurate (dotted) and in an inexact way (dashed).

The following example has been chosen in order to verify this segmentation approach by measurements. At first, a single SAW resonator was measured separately placed on a special metal carrier and using on-wafer probing. This device has been chosen as its input reflection coefficient covers a very wide range of values over frequency. Then, parallel to the resonator, the combination of substrate and package was measured as a four-port (once again in a special arrangement). Finally the overall circuit with the resonator placed into the package was measured, too. The overall measurements then were compared with the combined s-parameters from the measurements of the

separate parts (using lumped element bond wire models for their combination).

Fig. 7 shows the input reflexion coefficient of the resonator in a Smith chart. Excellent agreement is shown over the complete frequency range. In the considered frequency range, the input reflexion coefficient passes nearly the complete chart area.

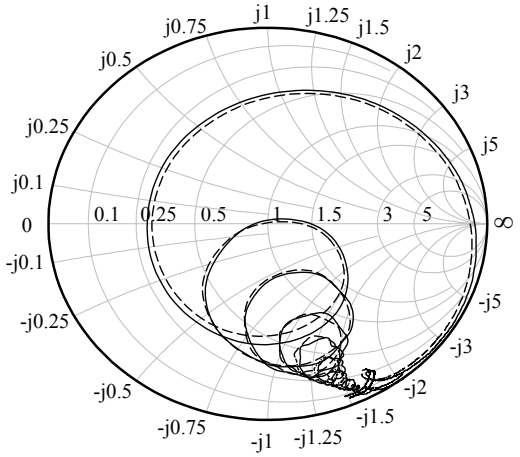

Fig. 7: Input reflection coefficient of packaged SAW resonator from 0.7 GHz to 1.1 GHz. Overall measurement (solid); measurement of PCB/ package and SAW resonator as single structures, the combined performance is calculated from the separate measurements (dashed).

C. Port selection / implementation of "lumped" circuits

As segmentation between carrier PCB and package leads to problems, PCB and package are simulated as a single unit, requiring considerable computational effort. Outer ports can be easily defined as standard planar transmission line ports or coaxial ports at the connectors are included in the simulation model. Inside a package, however, port definition is more complicated.

In reality, there usually exist bond pads to which the chip (MMIC or SAW filter) is connected using bond wires or ribbons. In special cases flip-chip bonding technique is used in order to avoid the spare area needed for classical bonding technique and so increasing the size of the packaged device. Thus, no well defined transmission line for a port definition exist.

Fortunately, most simulation tools include so-called discrete ports based on voltages and currents. In space-discretized time-domain simulators (e.g. FDTD), bond contacts and ground pads, forming the physical nodes of an internal port in a package, are separated by a number of discretization cells.

The discrete port itself is defined as a gap along the edge of a single mesh cell. The connection from the physical node - the bond pad or the ground pad in the simulation - to the port along the edges of the mesh is realized by an ideal, infinitely thin conductor (Fig. 8).

This conductor is formed in the simulation by setting the electrical field along the wire to zero. The conductor generates a parasitic inductance in the simulation, which does not exist in reality.

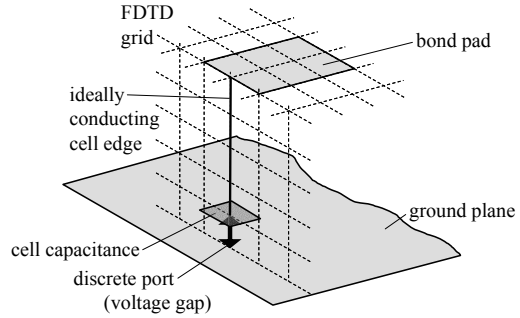

Fig.8: Position of a discrete port inside the simulation mesh.

A second parasitic effect in the simulation, connected electrically in parallel to the discrete port, is generated by the parasitic capacitance between the two parallel cell walls at the gap port.

To overcome these parasitic effects there generally exist two different methods. The first approach is based on the suppression of the appearance of the effect. This can be achieved by the usage of a distributed interface [11]. The method described here uses the calculation and compensation of the parasitic effects in a post-processing step. To this end, an effective radius of the mesh edges is computed. From this, an equivalent inductance can be derived which finally is used (with negative sign) to compensate its influence at the respective interconnect [12].

IV. Design and Optimization of New PCBs

In order to achieve an optimal design of test and application PCBs, the electromagnetic properties of all PCB parts have been precisely investigated. Furthermore, the electrical properties have been optimized towards neutral electrical characteristic of the PCB like:

- minimal reflections,
- minimal feed-through or cross-talk, and
- minimal losses.

Although geometric parameters have been carefully designed, fabrication tolerances result in large spreads and the need for prior verification. The optimized PCB parts described in the following can be combined in a modular approach.

The transition from the SMA connector to the microstrip line has been optimized to cause minimal reflections. Regarding Fig. 9, an improvement of around 20 dB has been obtained in the most relevant frequency range from 1 GHz to 2 GHz.

A variety of different landing areas for the SAW RF filter has to be handled, since the landing areas are designed according to the footprints of the packages as well as to the component's operation mode. In general, a good connection to ground for ground pads and a good shielding between signal pads implies the use of many vias between the top layer and the upper ground plane metalizations. The upper ground metallization is strictly kept solid. Details of such a landing area are shown in Fig. 10.

In another approach, the results gathered in the test PCB optimization have been transferred to a quasi-application PCB, i.e. the PCB in a mobile phone.

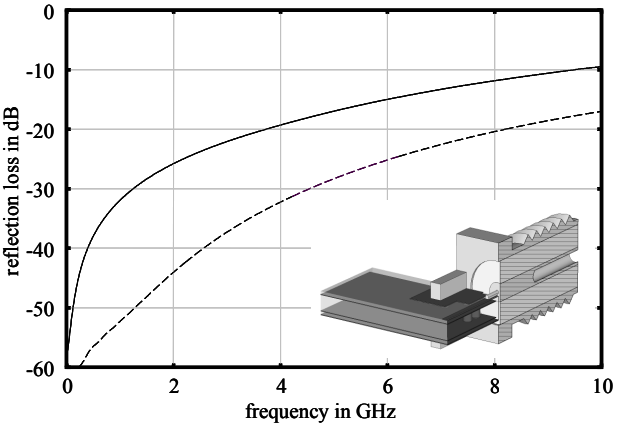

Fig. 9: Comparison of simulated return loss for an old (solid) and a new (dash-dotted, design shown in the lower right corner) transition from SMA connector to microstrip line.

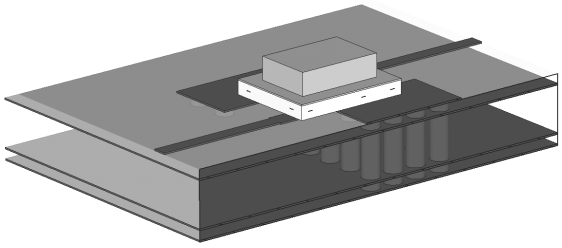

Fig. 10: Perspective view of the landing area extracted from a test PCB.

Due to the modified layer stack, the landing area had to be redesigned as described below. It should be noted that the height of the top dielectric layer of 60 µm is very similar to that of the phone PCBs and thus to the application environment.

The reduction of the layer height requires several changes in the landing area layout. Firstly, in order to achieve a characteristic impedance of the microstrip lines of 50 Ω, the line width has to be reduced from 340 µm to 100 µm. Secondly, a strong field discontinuity in the signal path is generated by the step in width from the microstrip line to the soldering pad. As a size reduction of the soldering pad is not possible due to the predetermined solder pad size of the SAW component and the positioning tolerances of the pick-and-place machines, an attempt has been made to reduce the effect of the discontinuity at the soldering pads by cutting out the areas in the ground layer immediately below the soldering pads. Thus, the second inner metal layer is used as the actual ground plane below the soldering pad.

Landing area designs for an optimized test PCB and an optimized quasi-application PCB are shown in Fig. 11a and Fig. 11b. As an example, a commonly used ceramic package of 3 mm × 3 mm size has been chosen.

The design aims at a uniform field distribution between the microstrip line and the package within the optimized landing area. In order to avoid field fringing and to guarantee optimal properties of the PCB, both size and position of the cut-out area have to be chosen carefully as indicated below.

The size of the cut-out area has to be realized in a way ensuring that the main part of the electromagnetic field lines

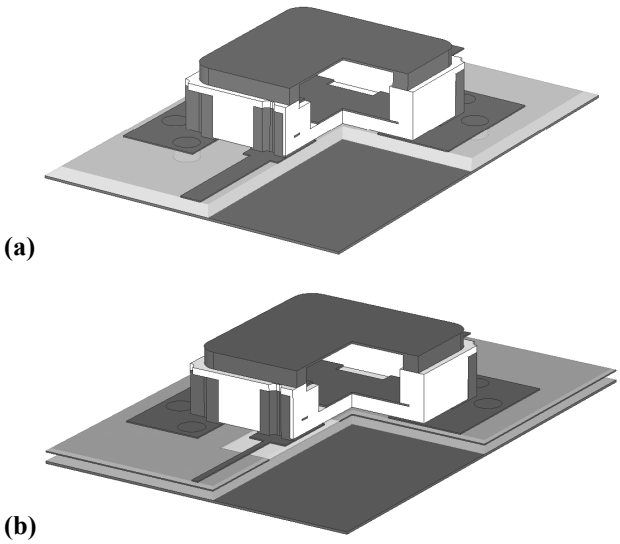

Fig. 11: Simulation models of the optimized test (a) and the new quasi-application (b) environment with mounted ceramic SAW filter package.

below the soldering pad go to the second ground layer. Thus, field components towards the edges of the cut-out in the upper ground layer have to be avoided. An undersized cut-out area will lead to almost unchanged field fringing as without cut-out.

Special focus has to be put on the front edge of the cut-out towards the microstrip. Its position must be chosen close to the soldering pad. Otherwise, an additional microstrip line with high characteristic impedance will be formed unintentionally by cutting away the original ground plane of the microstrip line, altering the properties of the SAW component. The result is a microstrip line of short length with very high characteristic impedance in the signal path, showing inductive behavior.

Another important point during optimization is the provision for an undisturbed current path. Hereto, a sufficient number of vias has to be positioned in the ground structures on top of the PCB in the vicinity of the microstrip lines, as shown in [3].

V. Results

For the purpose of validation, a SAW RF filter has been simulated and measured on both PCB structures as shown in Fig. 11. In Fig. 12 simulation results of this filter on the previous test PCB and on the new quasi-application PCB are given and compared to the corresponding measurements. The plotted curves indicate excellent agreement of the electrical characteristics with respect to stop-band and pass-band attenuation. Differences between simulation and measurement result from production tolerances of the PCBs.

Thus, the concept of a landing area design for application PCBs, having the same optimized electrical characteristics as on an optimized test PCB, has been proven.

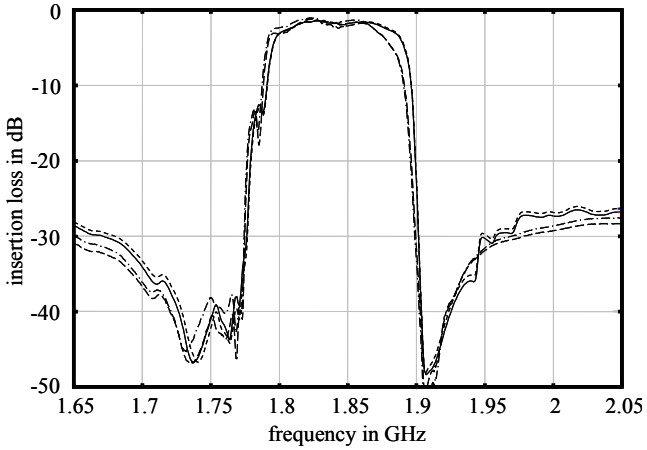

Fig. 12: Comparison of simulated and measured insertion loss of identical filters on an optimized test PCB (solid/ dash-dotted) and a new quasi-application PCB (dotted/ dashed).

VI. CONCLUSION

The paper has demonstrated a new concept of test PCBs showing that optimized PCBs for testing SAW RF components and optimized application PCBs for operating SAW RF components provide the same performance of the components. It has been proven that this is possible despite the fact that the two environments exhibit considerable physical differences regarding their layer stacks, for instance. The most important prerequisites have been the electrical properties of the PCBs, i.e., that the test PCBs show minimal reflections, minimal cross-talk, and minimal losses. In order to prove the concept, a quasi-application PCB representing the final phone PCB has been designed and evaluated. Therefore, a proposal for the landing area of an application PCB and, thus, for a phone PCB is given and discussed in detail.

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