Analysis and Design of a Frequency Synthesizer with Internal and External Noise Sources

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Abstract: In this paper we demonstrate a rigorous noise analysis of the PLL based synthesizer circuit. In contrast to analyses done previously, we are taking into account a more complete combination of noise sources. A second order PLL is used for this work. In contrast to the standard noise model, we choose an alternative model of describing noise. This leads to the derivation of a very general mathematical description for the output voltage, as well as for the output average power while taking into consideration noise sources at different points in the circuit. This mathematical description shows very clearly how the noise at different points in the circuit is changing the overall behavior of the synthesizer.

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INTRODUCTION

Today the design of a PLL based synthesizer including component selection and evaluation has become quite challenging. Many parameters must be evaluated. Among the crucial parameters is the phase noise, which is a random modulation of the phase of an oscillator's output due to a variety of internal and external processes.

In this paper we present a thorough analysis of the synthesizer based on a PLL circuit in order to study the effect of electronic noise coming from different sources from within the circuit as well as from the input signals. We represent the theoretical analysis methodology and after that we will follow up with presenting the results from simulations.

Many authors have done valuable studies on the noise behavior of a PLL using different models where they included some effects of noise [1]-[5]. We are continuing their work by doing an analysis of the noise in the synthesizer circuit taking into account the effect of additional noise sources.

NOISE ANALYSIS METHODOLOGY

A second order PLL is used for this work. As usual, it consists of a phase-detector (PD), a control filter (CF), and a voltage controlled oscillator (VCO). The control filter is described by the following transfer function:

$$F(s) = \left(1 + \tau_2 s\right) \Big/ \left(b + \tau_1 s\right) \tag{1}$$

A model for the output of the phase detector is used that does not only make possible to describe the influence of phase fluctuations, θ_i, but also those of amplitude

fluctuations, $R(t)$, in the input signal. Similarly, the locally generated VCO-signal will not only be described through its phase fluctuations, θ_o, but it also includes amplitude fluctuations, n'. The detector output voltage is thus described as a function, v_d, that depends not only on the phase-difference, φ, between VCO-signal and input-signal, but also on amplitude fluctuations of its input signals. The novel model shown below is thus more complete as compared to models in use:

$$v_d(t) = g\left(R(t), n'(t), \varphi(t)\right) \tag{2}$$

The noise sources under consideration here are the following:

1. Noise at the input of the PLL circuit, $n(t)$, which can be divided into two parts. A noise source $n_1(t)$ describing the phase variation of input and a noise source $n_2(t)$ included with $R(t)$ describing the amplitude variation of input.
2. The amplitude variations of the VCO signal, $n'(t)$, plays a role as a proportional term at the output of the phase detector, $v_d(t)$. It is designed in a way that it resembles this effect in a synthesizer circuit.
3. Noise source in front of the control filter, $n_3(t)$, is taken to be $1/f$ noise superimposed by white noise. The signal inside the loop is basically a base band signal, which can be expected to be affected by $1/f$ noise that is coming from different electronic devices in the loop.
4. Noise source in front of the VCO, $n_4(t)$, is designed to be a combination of $1/f$ noise and white noise.

The model used for the noise description can be represented by the following random process:

$$u(t) = \sum_{n=-M}^{M} A_n \cos\left(n\Delta\omega t + \varphi_n\right) \tag{3}$$

where $\Delta\omega := 2\pi/T_{ob}$ and T_{ob} is the observation time. This model is different from the standard used model, in the sense that the terms A_n are deterministic and the terms φ_n are random variables which are jointly uniformly distributed in the interval $[0, 2\pi)$. This less frequently used model can be traced back to S.O.Rice [6]. It is mathematically simpler and by virtue of central limit theorem it leads to the same results as the model that is more commonly used, anyway. The nonlinear differential equation of the PLL can be given by:

$$\tau_1\ddot{\varphi} + \left\{ b + K_o\tau_2 \frac{\partial g\left(R, n', \varphi\right)}{\partial \varphi} \right\} \dot{\varphi} + K_o g\left(R, n', \varphi\right) + K_o\tau_2 \frac{\partial g\left(R, n', \varphi\right)}{\partial R} \dot{R} = \tau_1\ddot{\theta}_i + b\dot{\theta}_i - b\omega_o \tag{4}$$

Since the mathematical analysis of a nonlinear differential equation is usually mathematically very complex, a novel linearization of the model is used. The phase detector function is linearized in the vicinity of operating point $\left(R_o, 0, \varphi_\infty\right)$. Here R_o is the amplitude of the input signal, φ_∞ is the steady state phase error, and φ_c is a constant phase shift of the input signal. The output of the phase detector can be described as:

$$v_d(t) = g\left(R, n', \varphi\right) \approx g\left(R_o, 0, \varphi_\infty\right) + \left.\frac{\partial g}{\partial \varphi}\right|_{\left(R_o, 0, \varphi_\infty\right)} \left(\varphi(t) - \varphi_\infty\right) + \left.\frac{\partial g}{\partial R}\right|_{\left(R_o, 0, \varphi_\infty\right)} \left(R(t) - R_o\right) + \left.\frac{\partial g}{\partial n'}\right|_{\left(R_o, 0, \varphi_\infty\right)} n'(t) \tag{5}$$

$$v_d(t) = g\left(R, n', \varphi\right) \approx \frac{b\Delta\Omega}{K_o} + K_D\left(\varphi(t) - \varphi_\infty\right) + K_A\left(R(t) - R_o\right) + K_V n'(t) \tag{6}$$

K_D, K_A and K_V represent phase detector gain, phase detector sensitivity to amplitude variation of input signal, and phase detector sensitivity to amplitude variation of VCO signal respectively. (Note the dependence on amplitude variation of the input and of the VCO). The following equation can be solved for the values of the operating points:

$$g\left(R_o, 0, \varphi_\infty\right) = b\Delta\Omega / K_o \tag{7}$$

where K_o is the VCO gain and $\Delta\Omega$ is the initial frequency offset between the input and the VCO. Taking the above discussions into account, the PLL based synthesizer model can be described by the following block diagram.

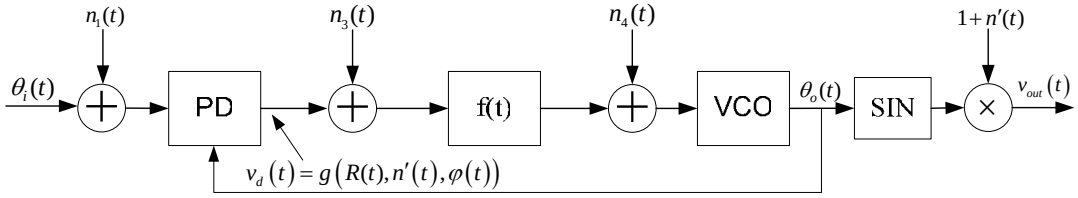

FIGURE 1. Synthesizer model used for the noise analysis.

Using the setup described above, an expression for the output voltage as well as an expression for the average power at the output were derived. Since they are rather complex formulas, they are not being presented in this paper. The calculations were done by taking into account noises at different points in the loop. The spectrum found was the general spectrum having influence of all noise sources described in this paper. The terms A_n from equation (3) allow for designing the noise to have that type of spectrum we want. The spectrum of the output was derived in terms of A_n of each noise source. This makes it a general description which can be designed to have a different type of noise at each point in the circuit.

SIMULATION RESULTS

The calculations were followed by simulations using SIMULINK where the noise sources are designed to represent the noise behavior at different points in a synthesizer circuit. The noise behavior was simulated using the nonlinear model with very satisfying results that show clearly how the noise at different points in the circuit affect the output of the synthesizer. Figure 2 represents the input and the output power spectrum of the synthesizer circuit with noise at different points of the circuit plotted on log-log scale. As it was expected from theoretical results (not shown here) the noise at different points in the circuit affects the system in different ways. Graphs (a), (b), (c) and (d) in Figure 2 show the spectrum of the output affected by amplitude variations of the input and the VCO, input phase noise, noise in front of loop filter, and noise in front of VCO respectively.

In the simulations presented here, the input noise is designed to be white noise that is divided into two components affecting the amplitude and phase respectively. All the random noise sources in this simulation are designed for SNR of -10dB. The angular frequency of the input signal is chosen to be $150\,Krad/\text{sec}$.

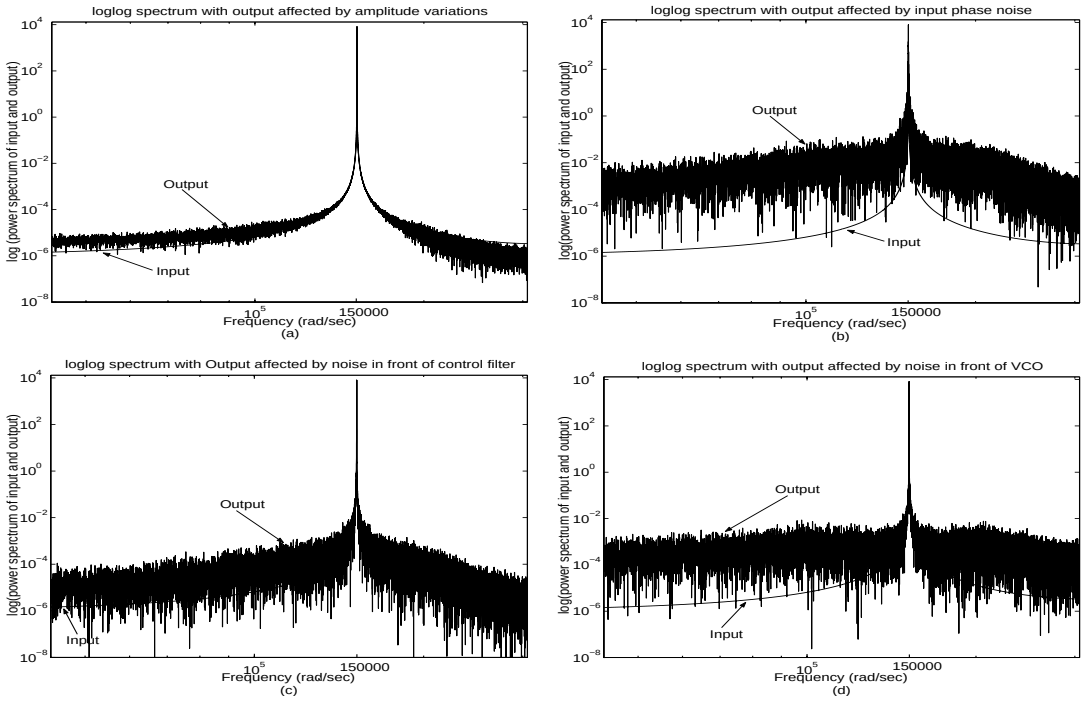

FIGURE 2. Graphs (a), (b), (c) and (d) show the power spectrum of the input and the output with noise present at different points of the circuit in Figure 1.

CONCLUSION

In this paper we have demonstrated the noise analysis of the PLL based synthesizer circuit taking into account a more complete combination of noise sources. A particular model of describing noise is used, which leads to the derivation of a very general mathematical description for the output voltage, as well as for the output average power while taking into consideration noise sources at different points in the circuit. This new setup leads to a deeper understanding of the complex noise phenomenon affecting the output of the synthesizer. It shows how each point in the synthesizer circuit is contributing to the overall noise behavior.

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