20th International Conference on Noise and Fluctuations, 14-19 June 2009, Pisa, Italy
AIP Conference Proceedings, Vol. 1129, pp.505-508, 2009

Experimental Study of Noise in a Frequency Synthesizer

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Abstract: This paper presents new results in the noise measurements of frequency synthesizers. Noise phenomena at the output of a synthesizer are very complex. Every component in the synthesizer contributes to the total output measured noise curve. Usually, it is not possible to separate the noise sources by just measuring the noise curve at the output of a frequency synthesizer. In this paper a technique is presented that can be used to investigate the noise contribution of different devices within the synthesizer. For this work, a synthesizer circuit is built and optimized to have a low noise floor. Then stronger noise is added at different points in the synthesizer in a way that it would represent noise of a certain device in the system, and that its provenance might be identified clearly. In advancement to the previous presentations, a very complex combination of noise sources is taken into consideration.

Keywords: Synthesizer, PLL, Noise Measurement
PACS: 01.30.Cc, 05.40.Ca, 02.60.Cb , 07.50.Ek,

INTRODUCTION

When designing a PLL based frequency synthesizer circuit, one of the important aspects to consider is the effects of electronic noise. The electronic noise coming from a variety of internal and external noise sources modulates randomly to the phase of an oscillator's output.

This paper contains a detailed noise analysis of a PLL based synthesizer circuit considering effects of internal and external noise sources. Theoretical analysis methodology and results from nonlinear simulations were presented by the same authors in [3],[4],[5]

NOISE ANALYSIS METHODOLOGY

The core of the synthesizer is a second order PLL (see Fig. 1), which as usual consists of a reference oscillator (XCO), a phase-detector (PD), a first order lag-lead control filter (CF), a voltage controlled oscillator (VCO), and a loop divider (1/N).

The noise behavior due to different electronic components within the synthesizer structure is considered through the design of appropriate noise sources. The additive noise sources shown in Fig. 1 represent the noise contribution of different components in the synthesizer. At the input of the PLL, the noise contribution n_i from the crystal oscillator as well as the noise n_M from the prescaler are considered. Inside the loop the additive noise n_{PD} of the phase detector, n_{CF} of the control filter, phase noise n_{VP} of the voltage control oscillator, as well as n_N of the loop divider are taken in to account.

In contrary to the commonly used model for the frequency divider consisting of a hard-limiter and a bandpass filter, a new superior model for non-ideal divider is already shown in the work published by the same authors in [4]. According to that model a non-ideal divider output signal would not only contain the phase noise of the VCO but it also contains a part of the amplitude fluctuations of the VCO signal.

In order to take into account amplitude fluctuations of the VCO signal, a four quadrant multiplier is used to modulate amplitude noise n_{VA} to the VCO output signal that is being fed back to the PD through the loop divider as shown in Fig. 1.

In the PD output signal $v_d(t)$ the terms $R_M(t)$ and $R_N(t)$ represents the effects of the XCO and the VCO amplitude fluctuations on the signal that is being fed back by the PD to the VCO. The nonlinear differential equation of this synthesizer system can be described similar to [3]. The analysis of such a nonlinear differential equation is usually mathematically very complex. The authors have already presented a novel linearization approach in [3].

The PD output signal in Fig. 1 shows that within the PLL bandwidth a part of amplitude fluctuations will be fed as tuning voltage fluctuations to the VCO input and will be converted into phase noise at the output of the PLL. This is also evident from the measurement results shown in Fig. 3(d).

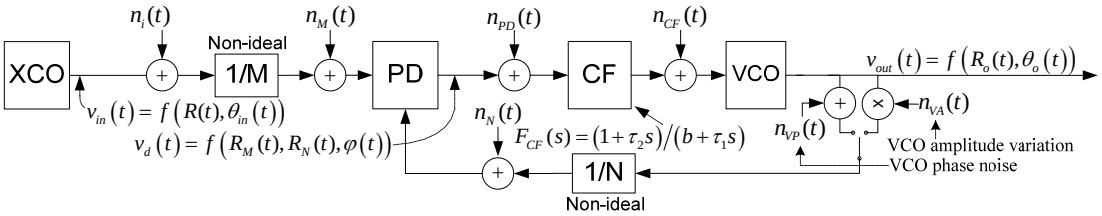

FIGURE 1. Synthesizer noise measurement setup block diagram.

MEASUREMENT RESULTS

In order to do an experimental study of noise, a frequency synthesizer circuit running at 10MHz is built. The synthesizer is based on Texas Instruments CMOS PLL chip SN74LV4046A. This chip contains a VCO as well as three different types of PDs; an XOR PD, a 3-state PD and a PD based on RS Flip Flop. Two separate chips are used; one for VCO and the other for PD. For the control filter both active and passive control filters are implemented. Measurements are done using XOR and 3-state PD as well as both active and passive filters. The results shown here are only for the 3-state PD and the active CF filter.

One of the important aspects when studying effects of noise on synthesizer is to find suitable circuits that will add noise to the PLL without influencing the dynamic behavior of the PLL circuit. Within the PLL loop active circuits based on operational amplifiers are used to add noise at different points in the circuit.

The output of the XCO and the VCO are digital signals that are first passed through bandpass filters in order to convert them into analog signals, and then noise is added. After noise addition the XCO and the VCO signals are passed through buffers (limiters) in order to convert them again into digital signal that is needed at the input

of the PD. As mentioned before, the multiplicative noise (AM noise) is introduced through the use of a four quadrant multiplier.

The measurements are preformed using the Rohde & Schwarz FSUP Signal Source Analyzer which facilitates achievement of accurate phase noise characterization of the system.

The power source for the PLL circuit is provided by the low noise regulator MIC5209. In addition to studying influences of noise within the PLL circuit, the effects of power supply noise on the XCO output is considered. For the XCO the DC supply coming from the regulator was passed through the buffer circuit shown in Fig. 2(a). As shown in Fig. 2(b) this lead to a noise level improvement of *+16dB* at 1kHz offset from center frequency.

The improvement in the noise performance is due to the fact that the operational amplifier has a high PSRR (power supply rejection ratio) which leads to a better noise and DC small signal variation rejection.

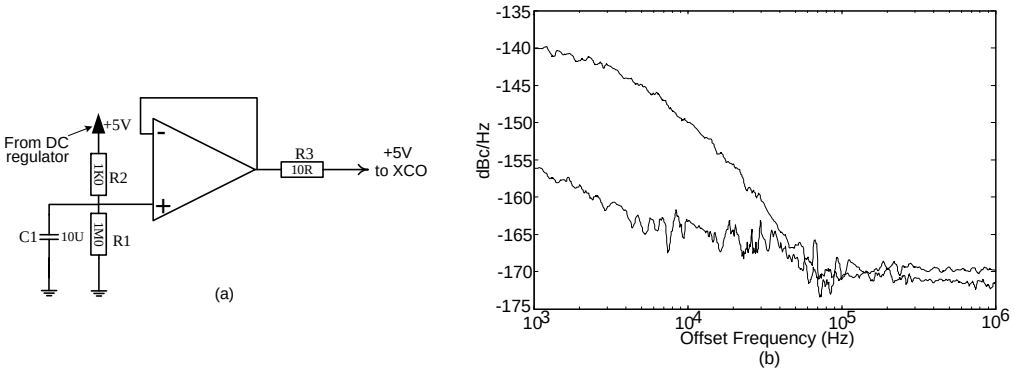

FIGURE 2. (a) XCO power supply with buffer stage; (b) SSB spectrum of the XCO output shows improvement in the noise performance after including the buffer.

Only some of the important results from the PLL noise measurements are shown here. Diagrams (a), (b), (c) and (d) in Fig. 3 show the single side band (SSB) phase noise power spectrum density of the synthesizer circuit with noise at different points. As it was expected from theoretical and simulation results (not shown here) measurements show clearly how the noise at different points in the circuit affects the output of the synthesizer.

A white bandpass filtered noise at the input of the PD (after XCO) causes a flatting of the output spectrum within the loop bandwidth as shown in graph (a). As expected the white baseband (low pass filtered) noise source inserted directly after the PD also causes a flatting of output spectrum within the PLL bandwidth, graph (c) shows that the PLL acts as a high pass filter for the white baseband noise, which is added directly after the CF (i.e. in front of the VCO). Graph (d) shows the measurement results, where a four quadrant multiplier was used to modulate baseband white noise (AM modulation) to the signal coming out of the VCO and which is fed back to the PD through the loop divider (see Fig. 1). The VCO amplitude fluctuations as expected do play a significant role in the output spectra forming. The amplitude fluctuations are converted by the PLL into phase noise, which appears in the output signal of the PLL as it is evident from Fig. 3(d).

CONCLUSION

This paper contains measurement results from a more complete noise analysis of a PLL based frequency synthesizer circuit considering a complex combination of noise sources. This new setup leads to a deeper understanding of the complex noise phenomenon affecting the output of the synthesizer. It shows how each point in the synthesizer circuit is contributing to the overall noise behavior. It gives deeper insight that can help in fine tuning the synthesizer circuit to reduce the total noise which appears in the output spectrum of the PLL signal.

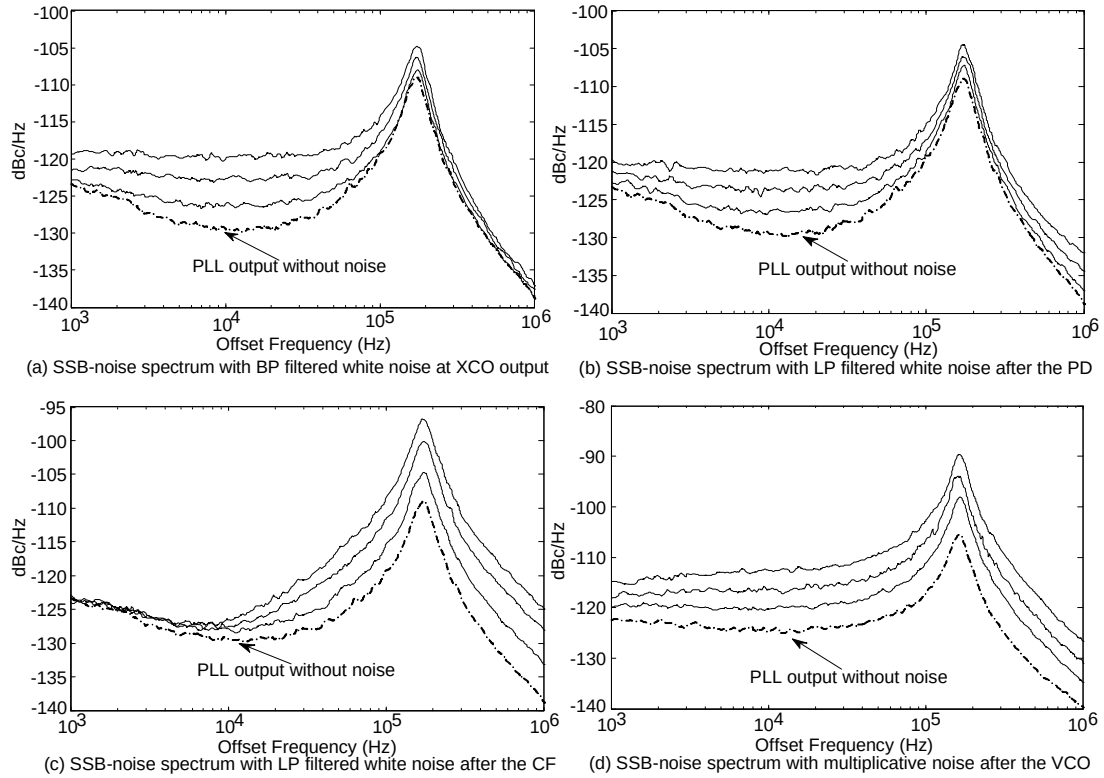

FIGURE 3. Graphs (a), (b), (c) and (d) show the single side band power spectrum of the output of the PLL with noise present at different points of the synthesizer.

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