Compact Bistatic 160 GHz Transceiver MMIC with Phase Noise Optimized Synthesizer for FMCW Radar

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***Abstract*—This paper presents an ultra compact bistatic FMCW radar transceiver MMIC at 160 GHz with a mixer-based synthesizer concept. The integrated mixer converts a ramp signal with a stabilized local oscillator (SLO) signal to the RF output signal. The usage of a mixer reduces the frequency multiplication factor of the ramp signal and hence improves the phase noise at 160 GHz. The fixed frequency local oscillator for the up-conversion has a comparably small phase noise level compared to the ramp input signal and does not contribute significantly to the total phase noise level at 160 GHz. Apart from the synthesizer, the MMIC also includes a power amplifier with a maximum output power of 2 dBm, two efficient integrated antennas with a wide radiation pattern, and an IQ-receiver. Two FMCW radar responses recorded with a bandwidth of 20 GHz show the dynamic range of this sensor and its near range behavior. The compact SiGe MMIC requires only a chip area of 1.4 mm × 1.0 mm and consumes 285 mW from a 3 V power supply.**

***Index Terms*—MMIC, FMCW radar, radar sensor, phase noise, SiGe.**

I. Introduction

The advances in the silicon-germanium (SiGe) technology [1] enable the integration of low-cost FMCW radar front-ends on an MMIC at frequencies above 100 GHz. Besides the costs, a crucial property for an FMCW radar is a low phase noise. Mainly two approaches for mm-wave broadband synthesizers are discussed in the literature. The first method uses integrated voltage controlled oscillators (VCOs), whose frequency is decreased with frequency dividers [2] to feed an external fractional-N PLL. The phase noise is reduced by the frequency dividers resulting in a low phase noise level at the phase frequency detector of the PLL. [3] demonstrate an offset fractional-N PLL with a mixer stage in the feedback path for an ultra wideband FMCW radar. The second method uses an off-chip ramp generation, where integrated frequency multipliers convert the IF to RF [4], [5]. This approach allows comparably large absolute bandwidths at RF with moderate tuning ranges for the VCOs that are used to generate the IF ramps. The disadvantage is the increased phase noise due to the frequency multiplication.

In this paper, a compact MMIC front-end with integrated antennas is presented, which is optimized for low phase noise through a mixer-based synthesizer approach. The required mixer input signals are a frequency ramp and a stabilized oscillator signal. The details of the 160 GHz MMIC architecture and the conditions for low phase noise are discussed in Section II. Afterwards, the phase noise behavior of the chip is characterized in Section III. Section IV contains the FMCW radar measurements showing the obtained SNR in a standard and a near range scenario.

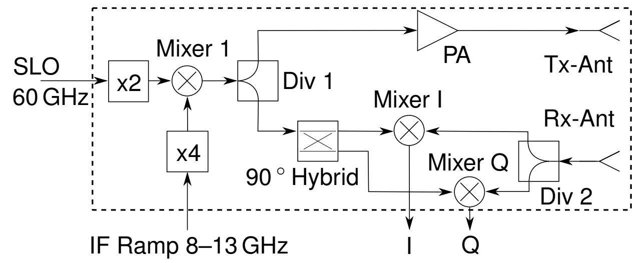

Fig. 1. Schematic drawing of the 160 GHz MMIC.

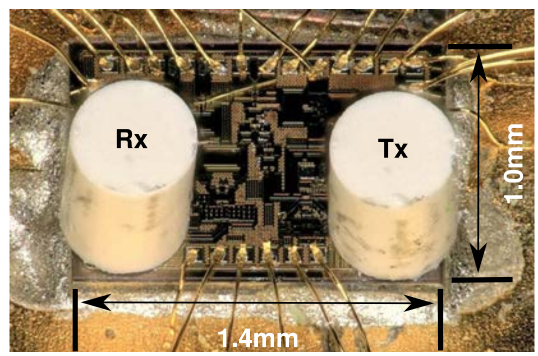

Fig. 2. Bonded MMIC with integrated antennas.

II. MMIC Architecture

Different approaches exist to generate a frequency ramp around 160 GHz from a ramp around 10 GHz. First, a frequency multiplication by 16 is possible, which, however, increases the phase noise by 24 dB. In this paper, the frequency multiplication is reduced to 4 reducing the phase noise degradation to 12 dB. This is achieved by using of mixer (see Mixer 1 in Fig. 1) in the synthesizer part of the MMIC, which converts the quadrupled ramp signal with a 120 GHz signal to RF. The 120 GHz signal is generated by a frequency doubler from an SLO-signal at 60 GHz. A 12 dB phase noise improvement compared to a frequency multiplication by 16 is only achieved when the SLO has a negligible phase noise

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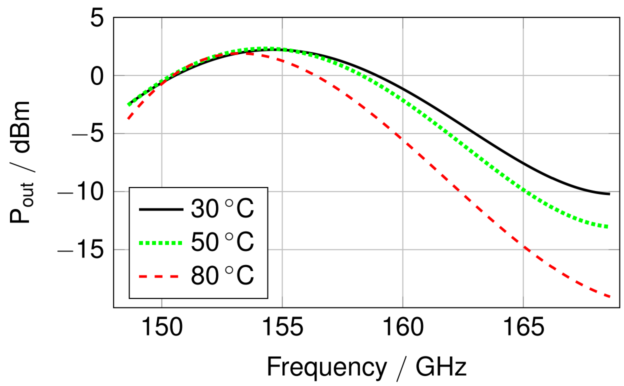

Fig. 3. Maximum measured transmit power after the power amplifier (PA) for different environmental temperatures. A polynomial fit of fourth order from 100 measured points was applied.

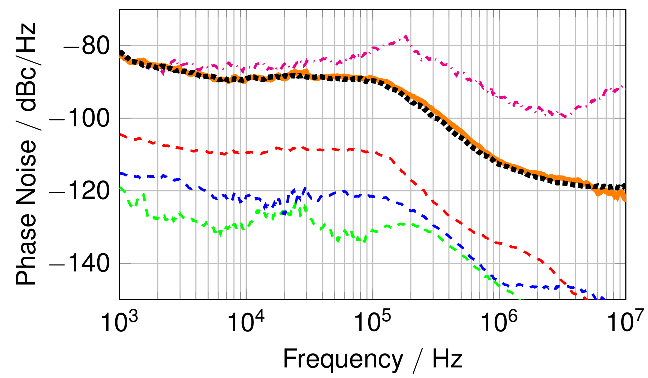

Fig. 4. Calculated (▬) and measured (▪▪▪▪▪▪) phase noise at 160 GHz, phase noise at 5 GHz of the three signal generators used to measure the phase noise at 160 GHz: PSG E8257D (- - -), PSG-A E8254A (- - -), and MXG N5183A (- - -), phase noise of the Hittite fractional-N PLL HMC703 with wideband VCO HMC588 at 10.5 GHz (-·-·-) used for the FMCW radar measurements.

in comparison to the ramp signal. This is true for this setup as shown in Section III. With this concept an RF ramp from 152 GHz to 172 GHz is created with an intermediate frequency ramp from 8 GHz to 13 GHz.

After Div 1 in Fig. 1 the transmit signal is fed to the power amplifier (PA), at which an output signal with maximum power of approximately 2 dBm was measured, as depicted in Fig. 3. The measurements were executed at three different temperatures. The results show a slight decrease of power for higher environmental temperature.

The integrated transmit and receive antennas have a shorted quarter wavelength line as a coupling structure on the chip, known from an 80 GHz antenna in [6], [7]. Unlike usually, where plastic or quartz glass plates with a patch radiator on top of the coupling structure are used, dielectric resonators as radiating elements with a diameter of 515 um, a height of 700 µm, and a permittivity of 10 were used. The dielectric resonator itself and the radiation mode are explained in [8]. With a simulated antenna efficiency above 50% and a gain of 6 dBi, a maximum EIRP of 8 dBm can be achieved. The simulated leakage attenuation between the antennas is higher than 20 dB due to the spacing in the H-plane of the antennas.

The receiver contains a hybrid coupler in the LO-path for IQ-generation, an active power splitter in the receiving path and the mixers for the conversion to baseband. The MMIC in SiGe technology with an f_T of 300 GHz and an f_{max} of 500 GHz draws 95 mA of a 3 V power supply resulting in a power consumption of 285 mW.

III. Phase Noise Measurements

For the measurements the ramp input was fed by a constant frequency from a signal generator. The SLO input is fed by a frequency doubled signal from a second signal generator. The 160 GHz RF signal was measured after the PA with a G-band probe. After the external down-conversion with a third signal source, the phase noise at 279 MHz was characterized and is shown in Fig. 4 as (▪▪▪▪▪▪). To evaluate this result the calculated phase noise at 160 GHz is added as (▬), which is based on phase noise measurements of the three used signal generators at a reference frequency of 5 GHz, additionally depicted in Fig. 4. As the phase noise level scales with the frequency multiplication factor, the three sources were multiplied with their respective multiplication factor, and added. The deviations of the measured and calculated phase noise curve are less than 1 dB up to 100 kHz and less than 2 dB in the whole frequency range. This demonstrates that the MMIC does not add phase noise in this configuration. Interchanging the three signal sources indicated that the external mixer, which is used for the down-conversion of the 160 GHz signal, has the largest influence.

For comparison, the phase noise of a fractional-N PLL with wideband VCO at the ramp center frequency of 10.5 GHz is added to Fig. 4 as (-·-·-). This confirms that the phase noise of the doubled SLO signal is negligible compared to the quadrupled ramp signal for the used radar setup. Consequently, an improvement in the ramp signal phase noise would lead to an improved RF phase noise.

IV. FMCW Radar Measurements

The radar measurements were performed with the sensor shown in Fig. 5. The setup is depicted in Fig. 6. The FMCW ramp signal for the MMIC is created with the above mentioned fractional-N PLL with wideband VCO. The SLO input is fed by a frequency doubled generator signal. The two integrated antennas illuminate a dielectric lens with a diameter of 37 mm. Due to the small distance of only 1.1 mm equal to 0.57 wavelengths between the integrated antennas, the tilt of the Tx-beam behind the lens compared to the Rx-beam is negligible. A corner reflector with a radar cross-section of 15 m^2 in a distance of 2.6 m was used as a target. The received IQ-signals were filtered with a 1 MHz low pass filter, amplified on the baseband board, and fed to the ADC. The ramp duration was chosen to be 500 µm. To reduce sidelobes a Taylor window was applied before the FFT.

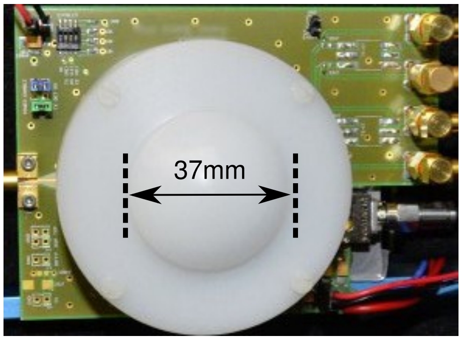

Fig. 5. Realized FMCW radar sensor with lens.

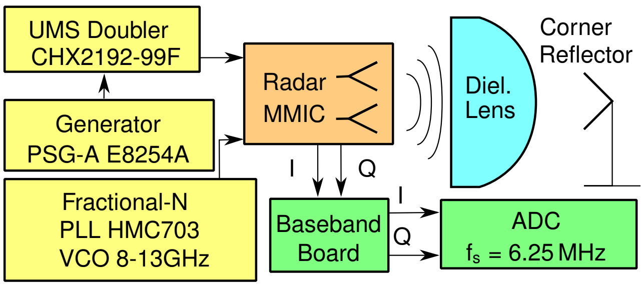

Fig. 6. Setup for the radar measurements.

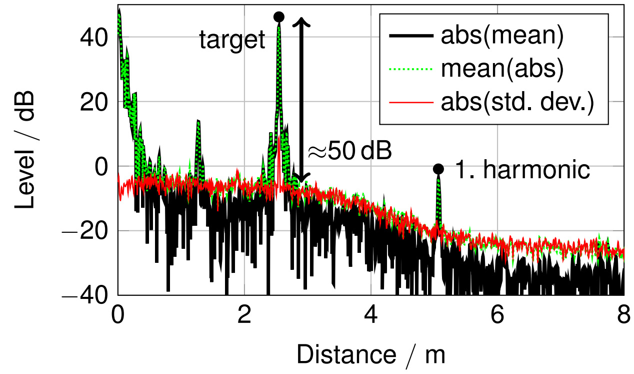

Fig. 7. Measured range response of the FMCW radar MMIC for an averaging of 10 measurements.

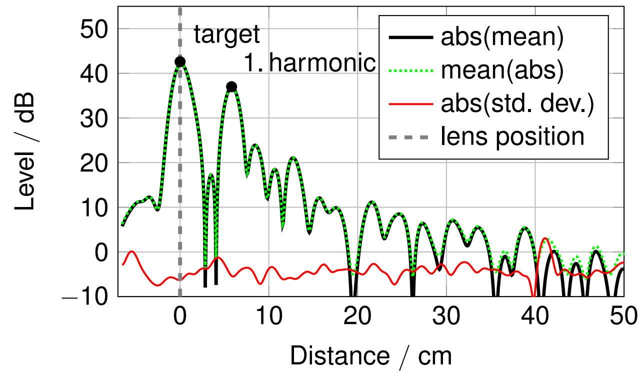

Fig. 8. Near range measurement of a 3 mm thick plastic plate directly in front of the lens with a complex subtraction of an empty radar channel response in the time domain, 10 measurements averaged.

A typical FMCW radar response measured with a bandwidth of 20 GHz is shown in Fig. 7. After the FFT of 10 measurement signals the absolute value of the mean, the mean of the absolute values, and the absolute value of the standard deviation are calculated for each range bin. Additionally to the target peak at 2.54 m with an SNR of about 50 dB, the first harmonic at 5.07 m is visible. The target position of a single measurement has a standard deviation of 24 µm for this setup, which is determined only from the amplitudes in the spectrum without phase evaluation. The ghost target at half target distance is created by the feed-through of a ramp with half bandwidth to the output of the quadrupler, which is up-converted by mixer 1 just like the desired ramp with full bandwidth. The amplitude of this ghost target peak is roughly 30 dB below the real target peak.

Figure 8 shows an FMCW radar response of a 3 mm thick plastic plate, which was positioned directly in front of the dielectric lens. Before the FFT a response calibration by complex subtraction of an empty channel response was executed. The target at the normalized zero position is clearly visible and has an SNR of about 48 dB. The first harmonic of the beat frequency appears at a distance of 5.7 cm corresponding to the electrical length from the MMIC to the lens surface.

V. Summary

In this paper a compact bistatic FMCW radar MMIC at 160 GHz with a mixer-based synthesizer architecture is demonstrated. The front end with the antennas is integrated on a chip area of 1.4 mm × 1.0 mm and has an EIRP of 8 dBm. The MMIC converts a ramp signal at an IF between 8 GHz and 13 GHz and a stabilized local oscillator at 60 GHz to the RF output signal with a bandwidth of 20 GHz. Using a mixer the frequency multiplier of the ramp signal is reduced, which results for a given ramp signal at IF in a better phase noise at RF in comparison to an approach with a pure ramp frequency multiplication. The phase noise measurements showed that the chip only scales the phase noise level of its input signals to the RF output signal and adds no additional phase noise. In the radar measurements a range precision of 24 µm was demonstrated at a distance of 2.54 m. In addition, targets directly in front of the lens were clearly detected.

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