Ultracompact 160-GHz FMCW Radar MMIC With Fully Integrated Offset Synthesizer

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(Invited Paper)

***Abstract*— The dynamic range of frequency modulated continuous wave (FMCW) radar sensors is often limited by the phase noise of the ramp signal. Especially at millimeter wave (mm-wave) frequencies, a low phase noise signal is very difficult to obtain. In this paper, a new system architecture, which is implemented in a low-cost, ultracompact FMCW radar monolithic microwave integrated circuit (MMIC) at 160 GHz, is proposed to address this topic. The approach is based on a frequency offset synthesizer, whose upconverting mixer is driven by a stabilized low phase noise local oscillator (LO) signal. This LO is generated by a fixed-frequency phase locked loop with a 2^N divider. The upconversion of the ramp signal with the stabilized LO signal leads to an excellent mm-wave phase noise of −89 dBc/Hz at a frequency offset of 1 MHz. By integrating the antennas on the MMIC, interconnects at mm-wave frequencies to package or printed circuit board are avoided and a simple assembly and interconnection technology is feasible. The ultracompact MMIC is realized on an area of only 2 mm^2, including the integrated antennas. A precision below 5 μm for range measurements is demonstrated with the radar sensor. Additionally, the radar performance is evaluated with two different voltage-controlled oscillators for the generation of the ramp signal.**

***Index Terms*— *D*-band, distance sensor, frequency modulated continuous wave (FMCW), integrated antenna, integrated phase locked loop (PLL), millimeter wave (mm-wave), monolithic microwave integrated circuits (MMICs), phase noise, radar system, SiGe bipolar.**

I. Introduction

THE increasing demand for low-cost and compact radar sensors pushes radar development to millimeter wave (mm-wave) frequencies. This is especially true for frequencies above 100 GHz, where entire radar front ends, including antennas, can be integrated on fast BiCMOS monolithic microwave integrated circuits (MMICs) [1]–[5]. Furthermore, the large bandwidth available at mm-wave frequencies provides high range resolution, which is required for short and medium range radars in automotive applications, level gaging, and medical sensing [6]. To successfully detect targets in complex scenarios, the dynamic range, which is crucial for the achievable signal-to-noise ratio (SNR), has to be optimized. In frequency modulated continuous wave (FMCW) radar systems, the dynamic range is often limited by the phase noise performance of the frequency synthesizer, which is used to generate highly linear frequency ramps. Several approaches for the FMCW ramp synthesis at mm-wave frequencies are known in the literature.

A simple approach is to use a voltage-controlled oscillator (VCO) that operates at mm-wave frequencies [7], [8]. A divider chain reduces its frequency to the range, where a fractional-N phase locked loop (PLL) that controls the VCO directly can be used for the ramp generation. Another approach generates the mm-wave ramp signal with a swept VCO at lower frequencies and a subsequent frequency multiplier chain [9], [10]. In both approaches, the ramp generation is based on digital circuitry working at comparably low frequencies below 1 GHz. Phase noise in this signal generating circuits scales with the square of the frequency ratio to the mm-wave signal, as both the multiplier and the divider chain can be regarded as frequency multiplication factors from a system perspective.

Promising alternative approaches toward low mm-wave phase noise are offset synthesizers, as realized in [11]–[13]. Downconverting mixers in the feedback loop are used to reduce the division factor in fractional-N-PLL-based synthesizers. If the fixed-frequency local oscillator (LO) signals contain reasonably low phase noise, the additional phase noise of the mixing process will be less than the phase noise saved from the decreased multiplication factor.

This paper follows the offset synthesizer concept and proposes a new system architecture for the mm-wave FMCW ramp signal generation, which is based on an upconverting mixer with a low phase noise LO signal. The schematic of the new system architecture with its building blocks is shown in Fig. 1 and discussed in Section II. In Section III, all building blocks of the realized MMIC, shown in Fig. 2, are characterized, including the integrated fixed-frequency PLL for the generation of the low phase noise LO signal, the upconverter for the ramp oscillator (RO) signal, the transmitter (Tx), the integrated on-chip antennas, and the receiver (Rx). The contributions to the total mm-wave phase noise are explained for two different ramp VCOs in Section IV. The sensor's

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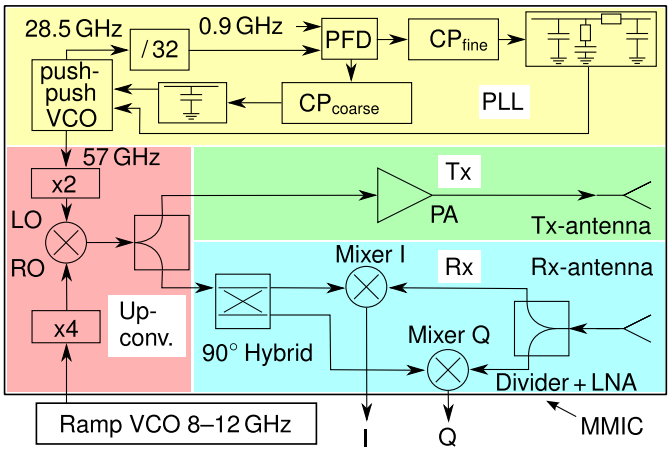


Fig. 1. Schematic of the radar MMIC with integrated offset synthesizer.

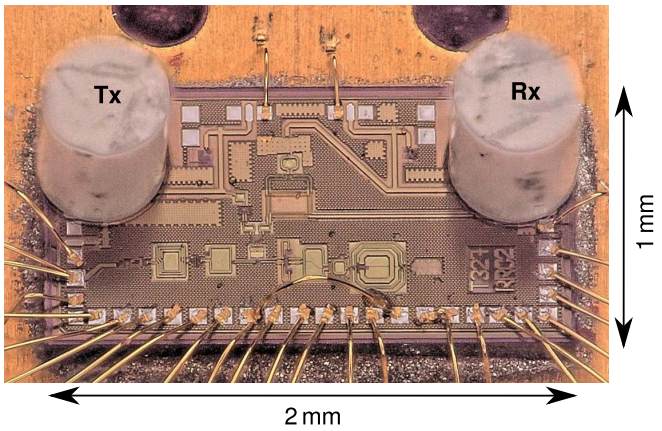


Fig. 2. Realized bonded die with chip-integrated DRAs.

radar performance is evaluated with three radar measurements in Section V.

II. System Concept

The proposed system concept uses a mixer for the upconversion of the ramp signal to the mm-wave frequency. If the fixed-frequency LO signal of the mixer has a small enough phase noise, it will hardly contribute to the phase noise of the mm-wave frequency signal at the mixer output. In the proposed architecture, the low phase noise LO signal is generated with an integrated fixed-frequency PLL with a 2^N-divider ($N = 5$). The underlying requirement for using a mixer with a fixed-frequency PLL and a 2^N-divider is that the signals from tunable PLLs with adjustable divider ratios have worse phase noise for a specific frequency. Additionally, VCOs with high Q-factors and very low sensitivities can be used in fixed-frequency PLLs. So, these PLLs are probably the best option for low phase-noise VCOs locked to a fixed reference. The lower the achieved phase noise of the LO, the higher its frequency should be chosen, to obtain the best dynamic range in the proposed FMCW radar with offset synthesizer. For broadband radars, however, the increase of RO frequency deviation is a consequence and might become another limiting factor.

In the presented MMIC, the ramp signal is between 32 and 48 GHz, which is then upconverted with a low phase noise LO signal at 114 GHz, as shown in Fig. 1. The frequency multiplication factor was reduced by 4 and the phase noise by 12 dB compared with a pure frequency multiplication from 10 to 160 GHz by a factor of 16.

Apart from the synthesizer part with the upconverting mixer and the fixed-frequency dual-loop PLL, the MMIC also includes a quadrupler, which multiplies by 4 the 8–12-GHz ramp input signal of the external VCO, to generate the ramp signal for the upconverting mixer. An active power splitter is used to divide the mm-wave signal at the output of the mixer into the transmit path and the LO path for the IQ-Receiver. The transmit signal is amplified in the power amplifier (PA) and radiated by the transmit antenna. The received signal is amplified in the LNA and divided for the IQ-Rx. The bistatic approach is chosen to reduce the leakage signal from the Tx to the Rx compared with a monostatic approach with an integrated Tx–Rx coupler. The lower leakage reduces the phase-noise-dominated noise floor and, consequently, increases the dynamic range of the radar. The two integrated antennas were positioned in adjacent MMIC corners with maximum separation, as shown in Fig. 2. By using small transformers and couplers, the realized radar MMIC covers only 2 mm^2, despite the bistatic approach with two integrated antennas.

III. System Building Blocks

A. Fixed-Frequency PLL

The design of the dual-loop PLL is based on a high phase frequency detector (PFD) frequency to reduce the overall frequency multiplication factor to the LO frequency at the upconverting mixer. As ultralow phase noise reference, a surface acoustic wave (SAW) oscillator can be used at 916 MHz. For that reason, the PFD operating frequency was set to around 916 MHz, and consequently, the reference signal can be fed via a standard bond wire to the MMIC. The PFD and the charge pumps (CPs) are realized with logic CMOS transistors of the BiCMOS technology. The two CPs convert the PFD output voltages into current pulses, where the coarse CP regulates the operating frequency of the VCO with a capacitor as an integrating loop filter. The fine CP ensures the phase lock with a third-order loop filter. The VCO operates from 28.5 to 30.4 GHz and is a push–push type oscillator, where the second harmonic of the common mode is taken as output. To close the loop, a divider by 32 is implemented in the feedback path of the dual-loop PLL. It is a master–slave toggle flip-flop circuit. The flip flop consists of two D-latches, implemented in a standard emitter-coupled logic [14]. A single differential emitter follower stage was used at every divider stage output to reduce the current consumption.

The phase noise of the PLL for the SAW oscillator at 916 MHz as reference is shown in Fig. 3 together with the reference and VCO phase noise. The phase noise curve of the locked VCO signal at the divider output shows a typical shape and has a phase noise of -135 dBc/Hz at 1 MHz.

B. Offset Synthesizer and Transmitter

The quadrupler in front of the mixer consists of an input balun and two differential push–push doublers. The upconversion of the quadrupled ramp signal is achieved by a Gilbert cell

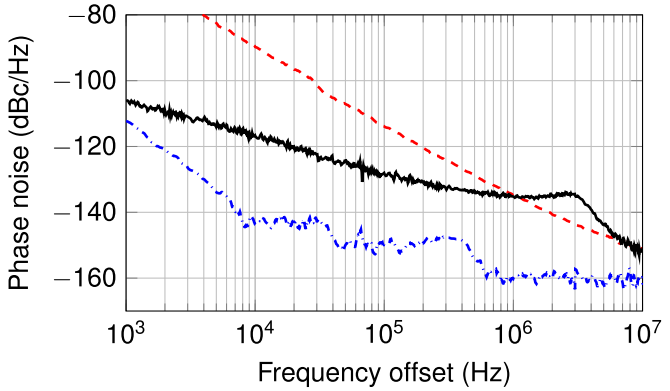


Fig. 3. Measured phase noise of the SAW oscillator (- · -) at 916 MHz, the free running VCO signal after the divider (- - -), and the PLL at the PFD input locked to the SAW oscillator at 916 MHz (——).

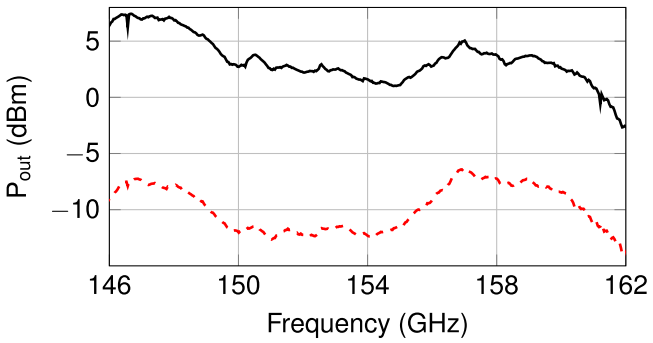


Fig. 4. LO power in front of the hybrid ring coupler (- - -) and PA output power (——) measured with a PLL reference frequency of 916 MHz.

mixer, which has no native sideband suppression. However, the following transformers, the PA, and the hybrid ring coupler in the LO path of the Rx have higher reflection coefficients and lower transmission coefficients for the lower sideband frequencies. Therefore, the signal path has an inherent filter characteristic. The main filters for the lower sideband suppression are the integrated antennas operating at 160 GHz.

After the upconverting mixer, the mm-wave signal is split in a cascade type differential amplifier, where each of the two output branches is fed into a balun. The first differential output signal is guided to the PA of the transmit path, the second to the 90° hybrid ring coupler to generate an I- and Q-LO signal for the Rx. The signal power in front of the hybrid ring coupler was measured with a probe tip and an auxiliary connection provided by using the focused ion beam technology. The output power from the PA over the mm-wave frequency was also measured with a probe tip and is shown in Fig. 4 together with the LO power in front of the hybrid ring coupler. The maximum LO power is −6 dBm and the average power about −9 dBm in the mm-wave bandwidth from 146 to 162 GHz. The output power of the PA reaches 7 dBm with an average power of 3 dBm. The variations of the output power are caused by the passive components. The transformer in the quadrupler has an undesired low-pass characteristic due to a slightly large inductance. Additionally, the transformer between the upconverting mixer and the power splitter is asymmetrical, which induces further fluctuations in the frequency response. In the radar measurement results in Section V, it will be shown that the effects of these fluctuations on the radar response can be significantly mitigated by using a calibration based on the Hilbert transform.

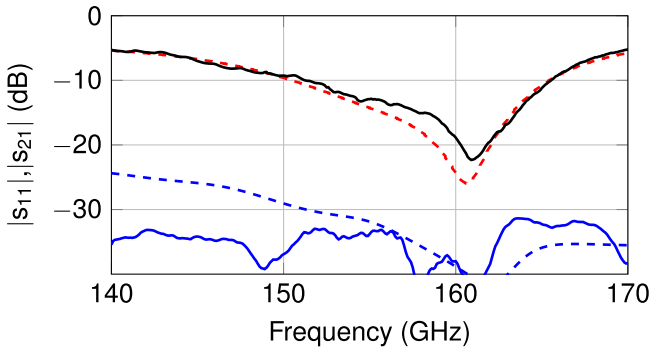


Fig. 5. Simulated (- - -) and measured (——) reflection coefficients and simulated (- - -) and measured (——) transmission coefficients between the on-chip DRAs.

C. Integrated On-Chip Antennas

The two antennas for the bistatic approach consist of a coupling structure in the back end of line (BEOL) of the chip and an external resonating element on top. The coupling structure is a compact short-circuited quarter wave transformer known from [15], [16] covering only 220 μm × 170 μm. It generates a strong electromagnetic field at the open end of the transformer, which couples to the resonating element. In general, two kinds of resonating elements are realizable. The first option is a patch radiator on a thin carrier substrate. Typically, quartz glass is used as a carrier substrate with a thickness of 75–127 μm, as shown in [15], [17], and [18]. The second option is a dielectric resonator antenna (DRA), which can be excited in the $\mathrm{TE}^x_{\delta 13}$ mode. In [19], the dielectric resonator and its radiating modes are explained with an excitation from an MMIC integrated half-mode cavity. Exciting the $\mathrm{TE}^x_{\delta 11}$ mode of the DRA with the short-circuited quarter wave patch leads to a strongly tilted main beam, which is not the case for the $\mathrm{TE}^x_{\delta 13}$ mode. Concerning the bandwidth, the $\mathrm{TE}^x_{\delta 13}$ mode is advantageous compared with higher modes like the $\mathrm{TE}^x_{\delta 15}$ mode.

The simulated and measured reflection coefficients of the coupled DRA in $\mathrm{TE}^x_{\delta 13}$ mode are shown in Figs. 5 and 6. The measured reflection coefficient of the integrated antenna fits very well to the simulation.

Due to the importance of the crosstalk from the Tx to the Rx in a bistatic radar, especially in an integrated radar front end on a very small MMIC, a BEOL-chip was processed to measure this crosstalk. On the BEOL-chip, the antenna structures were also positioned in two corners with the same distance as in the radar MMIC and were fed via mm-wave probe tips. The simulated crosstalk attenuation in the operating frequency range is higher than 25 dB and above 150 GHz better than 29 dB. In the measurements, the crosstalk attenuation is higher than 31 dB in the whole frequency range. This result emphasizes the advantages of the bistatic approach, which saves twice the insertion loss of an integrated

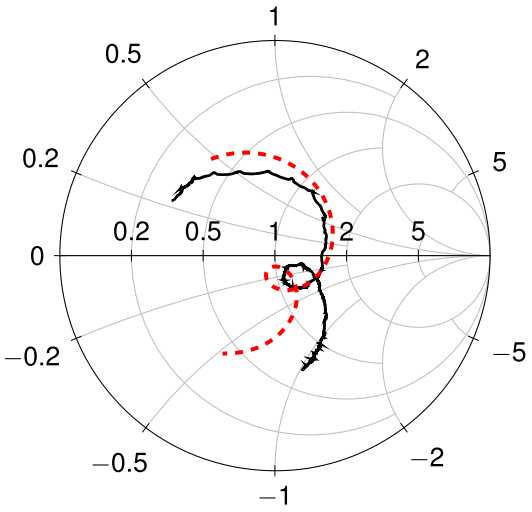
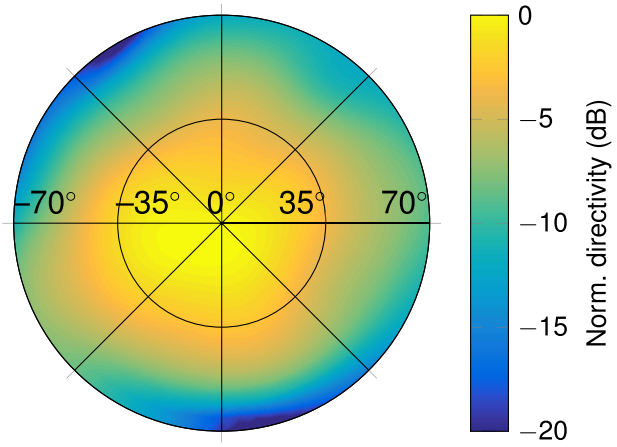


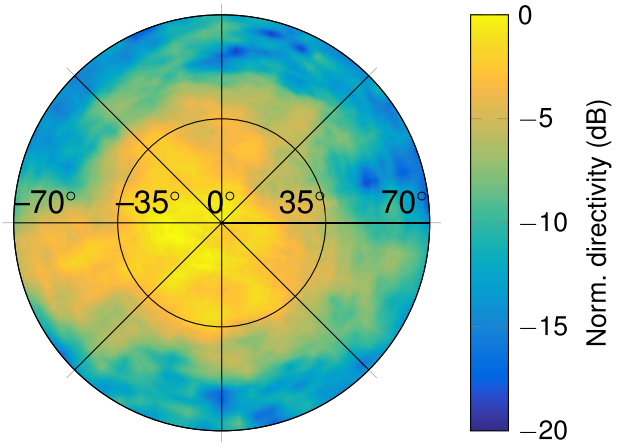
Fig. 6. Smith chart of the simulated (- - -) and measured (——) reflection coefficients of the on-chip DRA.

Tx–Rx coupler and has an excellent crosstalk attenuation. The crosstalk attenuation or leakage in FMCW radar systems typically determines the noise floor in the range spectrum and consequently the achievable SNR.

Due to the dielectric resonator on top of the MMIC, the electromagnetic wave can be radiated efficiently with a gain of approximately 6 dBi to broadside. The antenna has a simulated efficiency above 50%. The measurement of the 3-D-radiation pattern without probe tip is possible when the radar MMIC is fed with the respective signals to transmit a CW signal. The 3-D radiation pattern was measured with the automated measurement setup described in [20] and [21]. The simulated and measured 3-D radiation patterns are shown in Fig. 7. The simulation results of the integrated DRA show a smoother 3-D radiation pattern compared with the measurement result due to the limited modeling capabilities of the MMICs environment in the 3-D full-wave simulator. The bond wires and the shape of the ground pad, where the MMIC is glued on, are included in the simulation. However, the MMIC feeding lines on the printed circuit board (PCB) and the single layer capacitors are not considered in the simulation. This changes the lateral boundaries of the antenna simulation compared with the measurements. Additionally, further scattering centers on the PCB can lead to the obtained behavior in the 3-D radiation pattern. The measured 3-D radiation pattern of the integrated DRA has a 6-dB beamwidth of about ±40°. This emphasizes the robustness of the ceramic-based dielectric resonators in the proximity of bond wires, the silicon bulk, and the PCB environment. This radiation pattern is well-suited to illuminate a dielectric lens to enhance the antenna's directivity. A semiconvex lens was used, which was milled out of a PTFE (Teflon) block. The measured E-plane radiation patterns of the transmit and the receive antennas with a 37-mm-wide lens are shown in Fig. 8. The illustrated pattern of the Tx-antenna was positioned such that the maximum is at 0°. The homogeneous illumination of the on-chip DRA reduces the sidelobe level of the lens below −16 dB. The 3-dB beamwidth of the lens is 2.9°. With the formula of [22], the antenna directivity can



(a) Simulated normalized 3-D radiation pattern.



(b) Measured normalized 3-D radiation pattern.

Fig. 7. 3-D radiation patterns of the copolarization of the on-chip DRA on the bonded MMIC with evaluation board. The H-plane is oriented horizontally, the E-plane vertically, and scan of elevation angle from –70° to 70°.

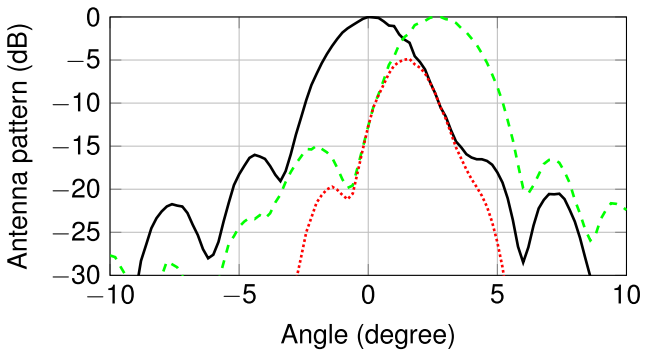


Fig. 8. Tx (——), Rx (- - -), and combined (·····) radiation pattern in the E-plane of the on-chip DRAs with a 37-mm-wide semiconvex lens.

be approximated by

$$G = \frac{32400}{\theta_{3\,\mathrm{dB}}^2} = 35.9\ \mathrm{dBi} \tag{1}$$

which fits to the theoretical value of 35.8 dBi calculated from the aperture size of the lens. The two-way radiation pattern is calculated as the multiplication of the measured Tx and Rx radiation pattern and is also shown in Fig. 8. The two DRAs

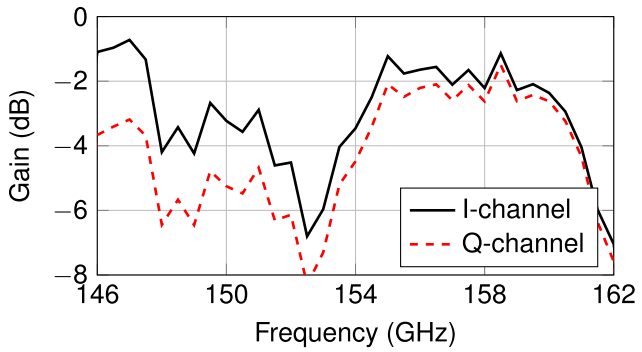


Fig. 9. Measured Rx gain of the I- and Q-channel over frequency.

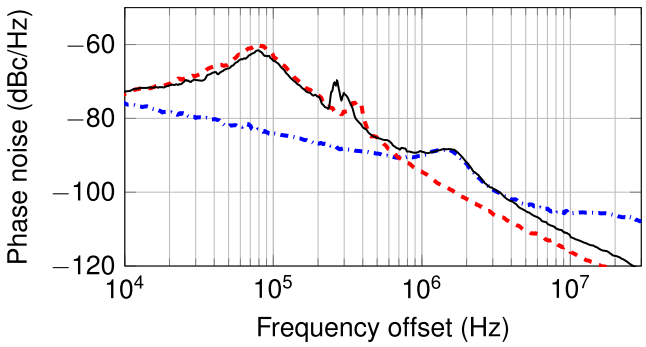


Fig. 10. Measured phase noise of the mm-wave output signal at 156 GHz for the SiGe VCO locked at 10.5 GHz (——), LO phase noise at mixer input calculated from the 891 MHz divider output measurement (– · –), and phase noise of the SiGe ramp VCO at the mixer input calculated from a measurement of the stand-alone VCO at 10.5 GHz (– – –).

are not on the optical axis of the converging lens because of their geometrical separation of 1.6 mm. The consequence is a tilt of the radiation pattern by 2.6° in the separation plane, which is the E-plane for this MMIC. The main beam of the combined radiation pattern is 5 dB lower compared with the theoretically achievable gain without any tilt. Hence, an increase of the lens diameter would not increase the two-way antenna gain, because the overlapping beam in the middle would be further attenuated by the multiplication of the two narrower single beams. The dependence of the main beam attenuation on the antenna separation is strongly nonlinear and with a distance of approximately 1 mm, the attenuation is below 2 dB. The radiation pattern in the H-plane is not affected by the antenna separation and as well-focused as in the E-plane.

D. Receiver

The Rx circuit is adapted from [23] and consists of an LNA, a mixer, and a 90° hybrid ring coupler in the LO path. The LNA is a cascode amplifier with a transmission line as load. The mixer is a double balanced Gilbert cell type with dc-current bypass for high linearity. The mixer employs a single transconductance common-base stage to supply I and Q. A transformer is used to couple the LNA and the mixer. The 90° hybrid ring coupler is based on a reduction of the quarter wave transmission line, as described in [24] and, therefore, covers only a chip area of 190 μm × 120 μm. The gain of the receiver from mm-wave input to baseband is shown in Fig. 9. The average gain is −3 dB with a maximum gain of −1 dB. The curve progression is similar to the measured LO power in front of the hybrid ring coupler in Fig. 4. This emphasizes the dependence of the Rx gain on the LO power of the mixer. For sufficient LO power, the targeted value of 2 dB could be achieved. The simulated noise figure of the Rx is 12 dB.

IV. MMIC Phase Noise and System Performance

For this MMIC, the ramp signal is created with an external VCO and fed into the MMIC at the ramp input around 10 GHz. This offers the opportunity to compare the MMIC performance for different ramp input signals in terms of phase noise and radar performance. In the following, a SiGe VCO operated from 10.4 to 12 GHz and the wideband VCO HMC588LC4 from analog devices operated from 8 to 12 GHz are compared. Both VCOs are swept by the same fractional-N PLL HMC703LP4 from analog devices.

The composition of the mm-wave phase noise is discussed on the basis of the SiGe VCO at 10.5 GHz. The upconverting mixer in the synthesizer part of Fig. 1 adds the phase noise of the two input signals. The phase noise of the integrated fixed-frequency PLL was measured at the divider output at 891 MHz. Consequently, the frequency multiplier is 128 to the LO frequency of 114 GHz at the LO input of the mixer. This means an increase of 42 dB compared with the measured phase noise at 891 MHz. The RO input of the mixer in Fig. 1 is fed by the quadrupled ramp input signal. The multiplication by 4 causes an increase of phase noise by 12 dB. The phase noise at 156 GHz at the mixer output could not be measured directly. The output signal of the PA was tapped using a probe pad and downconverted with an external converter module to 279 MHz, where the phase noise was measured. The LO signal for the external converter module was provided by a high performance signal generator to exclude phase noise contributions from the test setup.

The phase noise of the two mixer input signals, which was calculated with the respective multiplication factors and the measured data at the chip interconnect frequencies, is shown in Fig. 10 together with the measured phase noise of the mm-wave output signal. This result confirms that the MMIC itself does hardly add any further phase noise. As expected, the phase noise of the output signal at 156 GHz solely depends on the phase noise of the two mixer input signals.

The external SiGe-VCO around 10.5 GHz provides a comparably low phase noise for offset frequencies above 600 kHz. For that reason, the loop bandwidth was chosen below 500 kHz to achieve low phase noise at high offset frequencies. The phase noise response contains an undesired maximum at 80 kHz, which can be reduced with other loop filter settings. These loop filter settings might decrease the level of the unwanted maximum but could also increase the phase noise above 500 kHz. In general, the external loop filter of the fractional-N PLL can be adapted for specific scenarios. From a system's point of view, this superelevation is not desired, but is compensated to a certain extent by the phase noise cancelation for close range targets due to the correlation of the transmit

TABLE I
COMPARISON OF SiGe-MMICs ABOVE 100 GHz AND CMOS-MMICs FOR FMCW RADAR SYSTEMS

Reference	This work	[13]	[12]	[9]	[1]	[27]	[28]	Unit
Technology	SiGe	SiGe	SiGe	SiGe	SiGe	CMOS	CMOS	
Frequency	156	146	240	140	122	76	77	GHz
Bandwidth	16	48	61	14	9	1	1	GHz
Phase noise at 1 MHz offset	−89	−87	−84	−82	−100*	-85	-85	dBc/Hz
Transmit power at antenna input	5	−1	−1	4	4	5	-12 (VCO)	dBm
MMIC power consumption	360	650	5120**	724	900	243	51	mW
Antenna on chip / chip area	yes / 2.0	no / 3.863	yes / 2.851	no / 1.16	yes / 5.72	no / 1.045	no / 0.293	mm^2

* not sweeping
** complete sensor

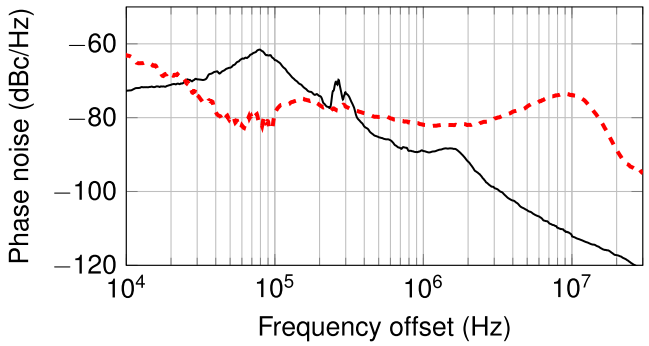


Fig. 11. Measured phase noise at 156 GHz for the wideband ramp VCO with active loop (– – –) and the SiGe ramp VCO with passive loop (——).

and receive signal in coherent FMCW radar systems [25], [26]. For larger distances, the phase noise cancelation decreases and, typically, also the signal level. Thus, a lower phase noise at higher offset frequencies is an option to increase the SNR for more distant targets up to 15 m. With this approach, a phase noise of −89 dBc/Hz at 156 GHz was realized at a frequency offset of 1 MHz.

The phase noise at mm-wave frequency for the second approach with the stabilized wideband VCO is compared with the mm-wave phase noise of the SiGe VCO solution in Fig. 11. The wideband VCO has a flatter characteristics from 30 kHz to 4 MHz, which is due to an active loop filter with higher bandwidth, which was fixed for this investigation. With a tuning voltage from 0 to 15 V, an active loop filter is required for the stabilization. As a consequence, the SiGe VCO provides better phase noise for distant targets and the wideband VCO for closer targets with the given loop filters configurations. From a systems point of view, the external PLL for the ramp signal generation is exchangeable. The performance of commercial PLL components, especially fractional-N PLLs, improves continuously. Thus, the systems phase noise can be improved with the progress of external PLLs.

The phase noise of the integrated fixed-frequency PLL was measured at the divider output to be −135 dBc/Hz at a frequency offset of 1 MHz. Consequently, −93 dBc/Hz is achieved at the LO input of the upconverting mixer by scaling the phase noise with its multiplication factor of 128 or 42 dB. Recently, MACOM presented new wideband VCOs with very low phase noise of −122 dBc/Hz at an offset frequency of 1 MHz in the frequency range of the ramp input signal. If these VCOs were used with the fractional-N-PLL, a phase noise of −93 dBc/Hz would be realizable with the proposed MMIC architecture.

The comparison to the state of the art for SiGe MMICs above 100 GHz is given in Table I. Concerning phase noise at a frequency offset of 1 MHz, an improvement was realized with the SiGe ramp VCO compared with other published work. The MMIC output power at the antenna input is similar to other reported work. With the mixer-based synthesizer approach, the VCO and the required frequency dividers for its stabilization at mm-wave frequencies are avoided. This is beneficial for the power consumption, resulting in a total power consumption of only 360 mW for this MMIC. The mm-wave bandwidth is approximately 16 GHz, which is limited by the bandwidth of the integrated antenna. Still, the integration of the antenna is very advantageous in terms of a low-cost assembly and interconnect technology. By integrating the antenna on the MMIC, no lossy mm-wave interconnects to package or PCB are required, which are often sensitive to fabrication tolerances. The short-circuited quarter wave transformers as feeding topology for the DRAs are not only an efficient method to radiate from a lossy silicon chip but consume only 220 μm × 170 μm of chip area each. Despite the extra area for the on-chip antennas, an ultracompact MMIC with a surface area of only 2 mm^2 was realized.

V. RADAR MEASUREMENTS

The radar measurements were performed in an anechoic chamber with corner reflectors as targets. A schematic of the setup is shown in Fig. 12. The radar MMIC can be fed by the wideband VCO from 8 to 12 GHz and the SiGe VCO from 10.4 to 12 GHz. The differential IF output signals of the MMIC are amplified and filtered on the baseband PCB and sampled with 4 MHz using a 12-bit analog digital converter (ADC). This setup allows ramp durations from 128 to 1024 μs. The evaluation of the sampled time signals involves the following steps. After removing the mean value from the sampled time signals, the envelope is determined by the Hilbert transform and is compensated. In order to use the radar in a multitarget scenario, the envelope of the time signal was first determined in a single target scenario. Since the envelope is almost not temperature-dependent and time-invariant, a calibration for the multitarget scenario can

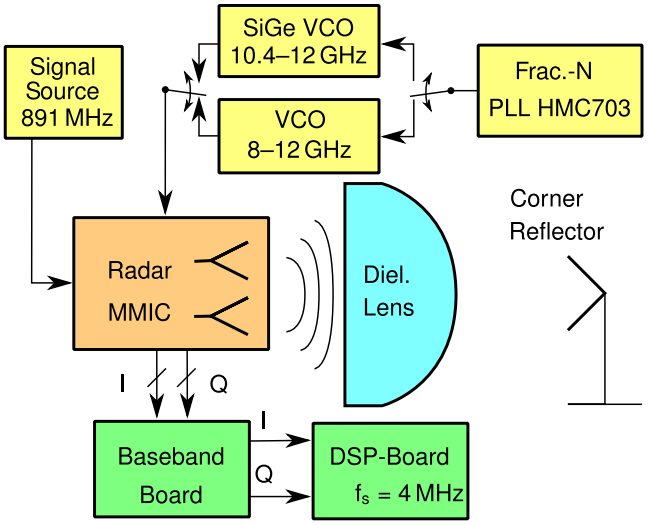


Fig. 12. Radar measurement setup with MMIC, signal generation, and back end.

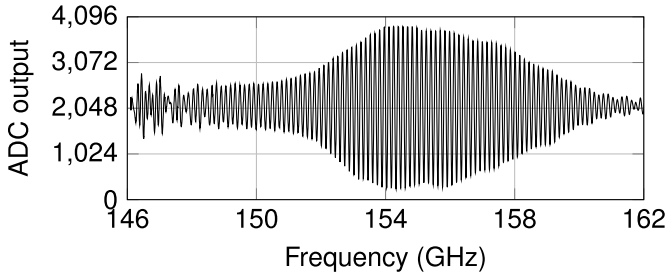


Fig. 13. Averaged IF time signal of 100 measurements for the radar measurement with a corner reflector in 1-m distance and 16-GHz RF bandwidth shown over the swept mm-wave frequency band.

then be performed. A Chebyshev window with a sidelobe suppression of 80 dB is applied to the time signal.

In the first FMCW radar measurement, a corner reflector with an edge length of 25 mm and an appropriate radar cross section (RCS) of −3.3 dBsm is chosen as target. The ramp signal is generated by the wideband VCO and has an mm-wave bandwidth of 16 GHz, swept in 1024 μs.

To demonstrate the optimum radar performance, the reference frequency for the fixed-frequency PLL on the MMIC was reduced from 916 to 891 MHz. The phase noise curves in Section IV were also measured with this adjustment. This frequency reduction results in a 3.2 GHz lower mm-wave frequency band compared with the reference at 916 MHz. This measure shifts the maximum IF amplitude to the middle of the IF time signal, as shown in Fig. 13. The frequency responses of the PA output power and the conversion gain of the Rx were both measured with the nominal PLL reference frequency of 916 MHz. Consequently, they fit better to the envelope of the IF time signal after the corresponding down shift by 3.2 GHz. The maximum of the IF envelope in the radar measurements corresponds to the second increase in the curves of the PA output power and the Rx gain. Above 159 GHz, the lowpass behavior of the first transformer in the quadrupler is responsible for the decrease of the IF amplitude. The first increase in the PA output power and conversion gain is shifted out of the operating bandwidth for the radar measurements,

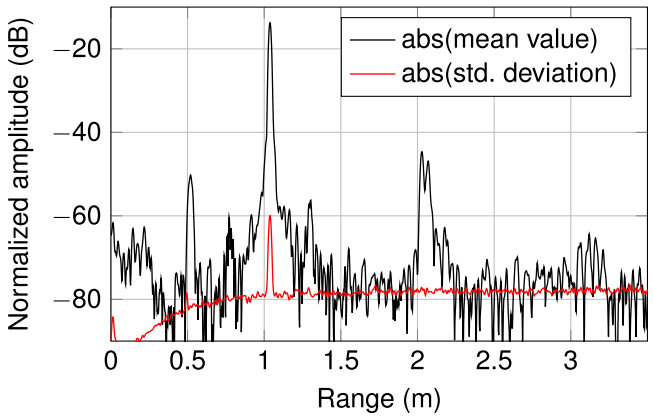


Fig. 14. Range spectrum of the IF signal for the radar measurement with a corner reflector in 1 m distance to the sensor and 16-GHz RF bandwidth.

since distortions caused by the second harmonic of the ramp input signal were comparably strong in this frequency range. From 146 to 148 GHz, these distortions are still visible in the IF time signal. The reason for this is the feed through of the second harmonic to the output of the wideband quadrupler. At the mixer, the undesired second harmonic of the ramp input signal is mixed in reverse frequency position with the third harmonic of the integrated fixed-frequency VCO at 171 GHz. This distortion can be suppressed by adding a low-pass filter between the doubler output of the fixed-frequency PLL and the upconverting mixer.

The 100 IF time signals were recorded and used for the spectral evaluation of the set of curves. For the determination of systematical errors in comparison to thermal noise or phase noise, the absolute of the mean value and the absolute of the standard deviation are displayed in the range spectrum in Fig. 14. The disturbances above the noise floor are caused by spurious signals, which deteriorate the time signal only at specific samples. These short-time distortions lead to an increased floor in the range spectrum, because they are almost coherent in all time signals. For that reason, the mean value of the range bins, which are located besides the target peak in the range spectrum, is higher than their standard deviation. In case of noise limitation, the mean value would be approximately 20 dB lower than the standard deviation besides the peak for an averaging of 100 measurements.

The target peak at 1 m is approximately 64 dB higher than the average noise floor in Fig. 14. The mentioned undesired second harmonic leads to a ghost target at 0.5 m due to its half ramp slope compared with the desired fourth harmonic. This ghost target is suppressed by 36 dB compared with the real target. The ghost target at approximately 2 m can be caused by multiple reflections between the target and the sensor or a harmonic signal due to a saturation of the Rx. It is suppressed by 30 dB compared with the real target. All ghosts are completely predictable and have no stochastic parts. Therefore, after the recognition of the strongest target, which is the real one, the position of the ghost targets can be predicted exactly.

The SNR of the real target of 64 dB results in a standard deviation of the target distance of 4.2 μm for the amplitude

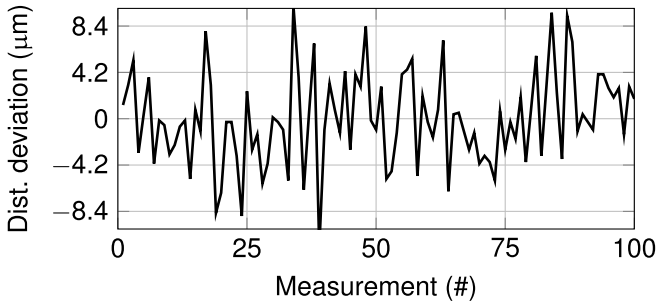


Fig. 15. Variation of the target distance for 100 measurements.

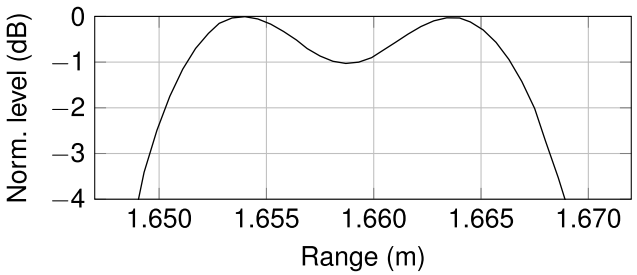
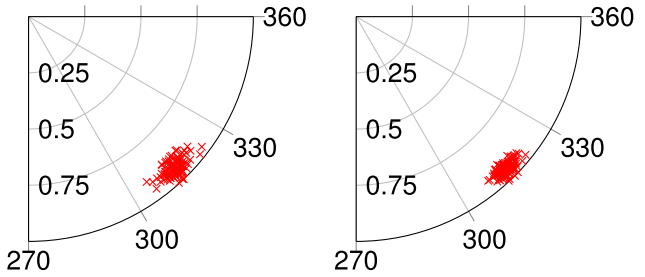


Fig. 16. Range spectrum of the IF signal for two targets close together in 1.65 m distance to the sensor and 16-GHz RF bandwidth.

evaluation. The deviations from the mean target distance for the 100 measurements are shown in Fig. 15. As one measurement was recorded per second, the total measurement time was 100 s, in which no drift of the deviations over time is perceptible.

The range resolution was determined in a second radar measurement with two corner reflectors of the same size. One corner reflector was moved stepwise until the two peaks were separated by a notch of 1 dB. The measurement result in Fig. 16 shows a separability of 9.7 mm with a rectangular window function. The smooth curve was realized with zero padding before performing the FFT. Theoretically, a range resolution of 9.4 mm is possible with a bandwidth of 16 GHz. The difference of the measured value to the ideal value of only 3% is very small.

The comparison between the wideband VCO and the SiGe VCO is performed in the second radar measurement. The wideband VCO is swept in the same frequency range as the SiGe VCO. The target of the third radar measurement is a larger corner reflector with an edge length of 99 mm and an RCS of 20.6 dBsm at a distance of 6 m from the sensor. An additional baseband amplifier with a gain of 22 dB was inserted to the optimal use of the ADC range. For the calculation of the range spectrum, the compensation of the envelope by the Hilbert transform was skipped. The complex phasors of the target peak in the range spectrum for 100 measurements for each VCO are depicted in the complex plane in Fig. 17. The amplitude of all phasors is normalized to the maximum absolute value of the 100 measurements. The point cloud of the wideband VCO is larger than the point cloud of the SiGe VCO. The distribution of the points is mainly spread in the angle direction, which is due to phase noise. As explained in Section IV, the ramp synthesis with the



(a) Wideband VCO with active loop filter (b) SiGe VCO with passive loop filter

Fig. 17. Comparison of the complex phasor at the target position in the range spectrum for 100 measurements of two different ramp VCOs feeding the front-end MMIC.

wideband VCO has a higher phase noise at larger frequency offsets. The consequence in terms of precision in this example is that the wideband VCO reaches a precision of 0.5 mm and the SiGe VCO a precision of 0.4 mm. Besides the benefits concerning assembly and interconnect topics, additionally, the integration of a SiGe VCO creates the degree of freedom to use an active or passive loop filter. In contrast, the wideband VCO with a tuning range from 0 to 15 V requires generally an active loop filter design, which can be disadvantageous in terms of phase noise and radar performance.

VI. Conclusion

In this paper, a novel radar system architecture with a phase noise optimized synthesizer concept implemented in a very compact, low-cost MMIC has been shown. The mixer-based offset synthesizer enables a state-of-the-art phase noise performance at mm-wave frequencies by mixing an intermediate frequency ramp signal with a low phase noise LO signal to the mm-wave frequencies. This approach realizes a phase noise of -89 dBc at 1 MHz, which is beneficial for more distant targets. Additionally, the low-cost radar sensor was evaluated for closer targets showing a precision better than 5 μm.

With the antenna integration on chip, no mm-wave frequency interconnects have to be implemented resulting in a simple and cheap assembly and interconnect technology. By additionally integrating the wideband VCO around 10 GHz on the MMIC, the reference clock at 916 MHz for the integrated PLL is the highest frequency that has to be bonded to the MMIC and guided on the PCB. Consequently, lossy materials like FR4 can be utilized for the PCB realization. The technical feasibility of the integration of a wideband VCO in SiGe technology has been demonstrated amongst others in [11], [29], [30].

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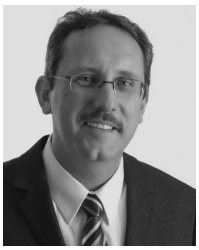

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