A Modular Phased Array Transceiver with RF-MEMS SPDT switches in a 0.25 µm SiGe BiCMOS Technology

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***Abstract*—An highly-integrated active reflectarray transceiver enhanced with fully monolithically integrated RF-MEMS SPDT switches is presented. The system operates at Ka band and follows a 3-D manifold concept incorporating wide angle scanning antenna elements, RF interconnects, mixed-signal MMICs in a flexible and scalable manner. Apart from this, the thermal management of the system, as well as the robustness and reliability of RF-MEMS SPDT switches are discussed. To verify the technological methodology, a phased array demonstrator with 144 elements has been realized demonstrating excellent scanning performance up to 60° from boresight.**

***Index Terms*—Phased array, Ka band, MMIC, RF-MEMS.**

I. Introduction

In the recent years, there has been a continuously growing interest in satellite communications at Ka band. This trend is mainly driven by the necessity of ever higher data throughput rates and comes along with the demand for miniaturized antenna terminals in mobile scenarios. Especially on highly dynamic platforms such as airplanes, low-profile and lightweight phased array architectures are more favorable than their mechanically scanning counterparts. Meanwhile, phased array systems using SiGe MMICs may offer a feasible and affordable solution to keep established communication links while the platform is moving rapidly.

Therefore the underlying system architecture employs the concept of a folded reflectarray antenna [1] with T/R functionalities for the 29.5 GHz to 30.8 GHz frequency range. By means of the proposed space-fed arrangement, a complex and lossy RF distribution network can be avoided. In contrast to conventional approaches [2], a mixed-signal MMIC with RF-MEMS SPDT components is used to overcome switching losses in the millimeter wave regime. The MMIC demonstrates the combination of Si/SiGe HBTs with RF-MEMS, on chip DC/DC converters, mixed-signal and mm-wave circuit blocks. To the authors' best knowledge this paper presents the first active phased array system with monolithically integrated RF-MEMS SPDT switches at millimeter wave frequencies

II. Module Architecture

Since phased array antenna systems in the millimeter wave regime typically have a very high packaging density, a 3D-integration concept for the module architecture has been chosen to integrate all required components within the confined space. Based on a state-of-the-art multilayer PCB, the layer stack up of the manifold is shown in Fig. 1. Moreover, advanced fabrication techniques such as stacked, plugged and back-drilled vias have been incorporated into the design process to improve the RF performance of the planar circuits by lowering the thickness of the individual metal layers. The multilayer configuration can be divided into 3 function parts. Layer (L7)-(L11) contain the radiating elements and their vertical feeding structures to the MMICs. The distribution layers on (L4)-(L6) are used to guide the DC and digital control signals to the chips. The active circuits and additional structures for optimal heat removal are integrated on (L1)-L3). Vertical interconnects between the metal layers are realized by different kind of via connections.

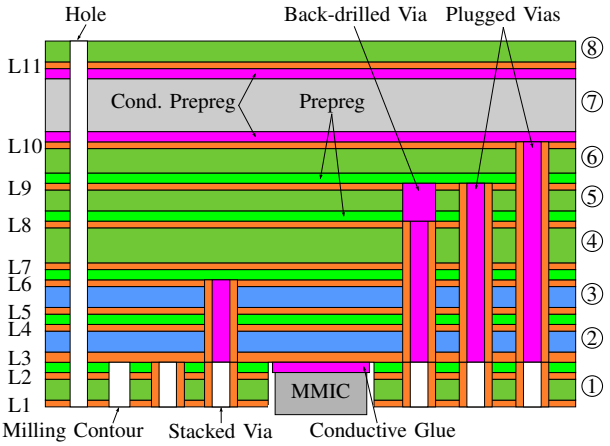


Fig. 1. Stack up of the multilayer PCB for the active phased array transceiver.

III. Antenna Element

In order to cover a large scan volume with the planar phased array system, the unit cell size should be kept small. On the other hand, the packaging density must be sufficiently low enabling the integration of any other components required. As a good compromise between those two aspects, the antenna

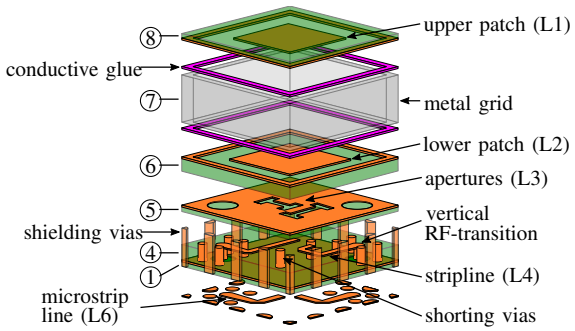
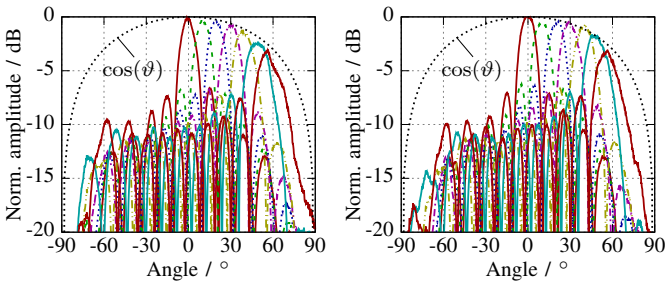


Fig. 2. Exploded view of the dual-polarized aperture coupled stacked patch antenna [3]; Layer ② and ③ for the distribution of DC and control signals are not shown here.

spacing is set to l_{uc}=5 mm using a non-skewed square lattice. The exploded view of the dual-polarized stacked patch antenna is depicted in Fig. 2. The deployed antenna design is subdivided into 3 parts to relax the technological requirements [3]. In this hybrid antenna configuration, the dielectric layers ① to ⑥ accommodate the lower microstrip patch and two H-shaped slots fed by stripline for each polarization. The stripline is again connected with the respective microstrip line on the outer layer by using an integrated vertical RF transition [4]. Furthermore, the unit cell is surrounded by ground vias to improve the shielding between adjacent elements. The upper microstrip patch on the thin RF laminate ⑧ is electromagnetically coupled to the lower one. The metal grid in between both square patches is used to adjust this coupled resonance. In addition, mutual coupling is reduced and the large air volume below the upper patch contributes to an increased operational bandwidth.

Based on the dual-polarized stacked patch antenna element, a 11×11 array prototype has been designed to validate its scan performance within an array environment. As this passive array configuration is used to validate experimentally the scan performance of a fully excited array by means of the embedded element pattern, only the two ports of the central element are fed. Fig. 3 illustrates the measured embedded element pattern superimposed with the array factor. As can be seen, the predicted scanning behavior in both the E- and H-plane



(a) E-plane (b) H-plane

Fig. 3. Scan performance of a 11×11 antenna array based on the measured embedded element pattern of the dual-polarized stacked patch antenna (port 1).

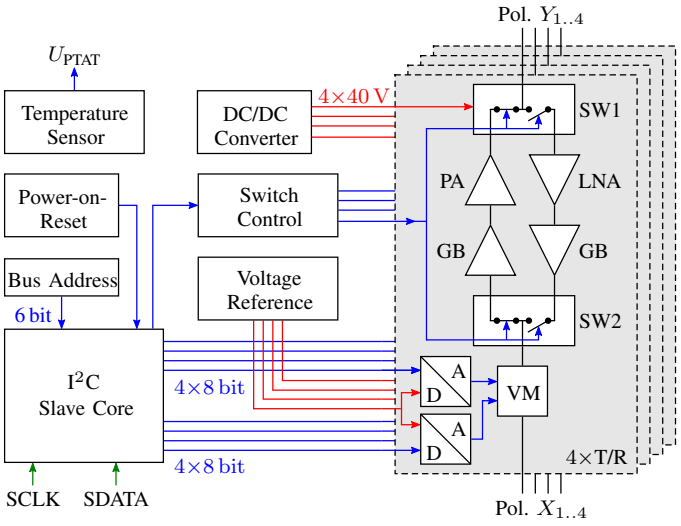


Fig. 4. Block diagram of the multi-functional MMIC with monolithically integrated RF-MEMS SPDT switches (SW1=RF-MEMS, SW2=nMOS).

are very close to the ideal $\cos(\vartheta)$ gain degradation indicating the antenna's excellent operability within the intended scan volume of $\pm 60°$.

IV. SiGe BiCMOS MMIC with RF-MEMS SPDT Switches

A functional block diagram of the developed MMIC is shown in Fig. 4. The underlying technology is based a 0.25 µm SiGe:C BiCMOS process from IHP Microelectronics enabling the monolithic integration of RF blocks, digital and mixed-signal circuitry, and even RF-MEMS switches [5]. The capability to combine all those functionalities into one multi-functional IC is a key aspect to overcome the demanding integration density of phased array systems at millimeter frequencies.

Owing to the small array lattice, four transceiver modules are integrated per MMIC [6]. Each of them contains a bi-directional vector modulator (VM), a power amplifier (PA), a low-noise amplifier (LNA), and two gain blocks (GBs). The direction of the signal flow between port X and Y is controlled by two SPDT switches. Since insertion loss at port Y has a crucial impact on the receiver noise figure, an RF-MEMS SPDT switch (SW1) has been deployed there. The other switch (SW2) is in a part of the circuit where switch loss is less critical, and this a conventional nMOS SPDT switch is used to conserve chip area. An integrated I²C slave core shared by the 4 T/R modules allows serial control of all MMIC functions and thus reduces the wiring density on the module level significantly. By using two 8 bit-DACs to control the vector modulator of each T/R module, the amplitude/phase constellation of the RF signal can be adjusted very precisely. Furthermore, all T/R module have a switch control, a power-on-reset block, a voltage control, a DC/DC converter, and a temperature sensor in common.

Fig. 5 illustrates the general cross section of the RF-MEMS switch with silicon (Si) cap packaging. As can be

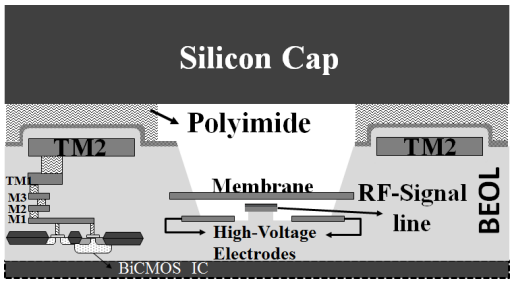
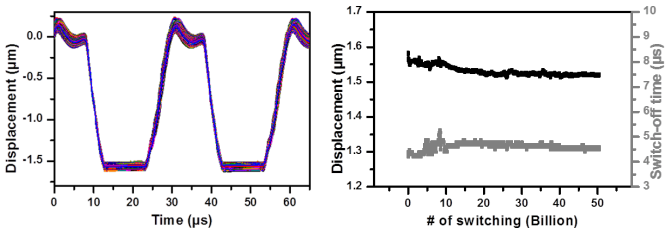
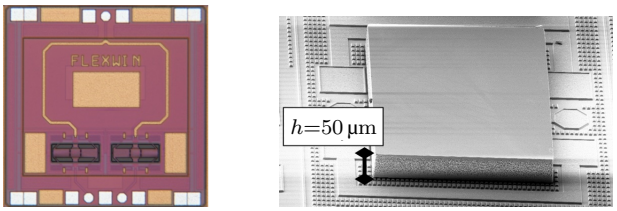


Fig. 5. Detailed cross section of the enclosed RF-MEMS SPDT switch [7].



(a) Displacement versus time (b) Overall displacement data

Fig. 6. Initial reliability test of the RF-MEMS switch.



(a) Micrograph (without Si cap) (b) SEM image (with Si cap)

Fig. 7. Fabricated RF-MEMS SPDT switch with non-hermetic encapsulation.

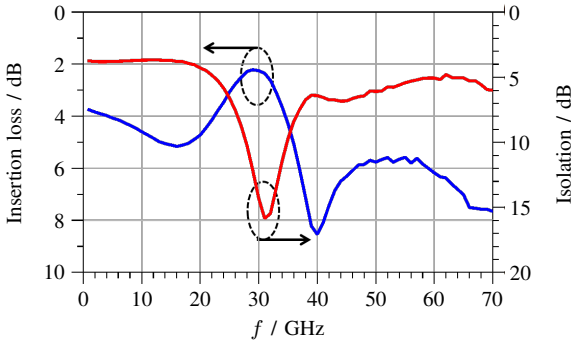


Fig. 8. Measured insertion loss and isolation of the RF-MEMS SPDT switch.

seen, the 0.25 µm BiCMOS technology provides 5 aluminum metalization layers in back-end-of-line (BEOL) process. The RF-MEMS switches are formed between the metal layer (M1) and (M3) of the BEOL [7]. A stress compensated metal layer (M3) is used to realize the suspended layer of RF-MEMS switch and metal layer (M2) is used as the RF signal line of the device. The actuation electrodes at which the high voltage is applied are realized using the metal layer (M1) of the BiCMOS process. A thin Si_3N_4/TiN stack, which is part of the BiCMOS metal-insulator-metal (MIM) capacitor, forms the contact region and provides DC isolation between the grounded membrane and the RF-signal line. After the MEMS releasing process, the RF-MEMS cavities are sealed with the Si caps at wafer-level. The applied wafer-to-wafer packaging technique is independent from the size of the Si caps; thus the packaging of several RF-MEMS switches can be realized at the same time. The high throughput and flexible size Si caps make it possible to provide BiCMOS embedded RF-MEMS switch technology with a non-hermetic packaging.

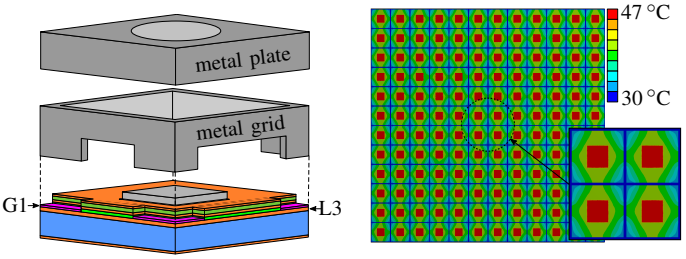
Initial reliability tests of the RF-MEMS switches have been conducted using 12 test switches in parallel [8]. The switches were cycled up to 50 billion cycles and the displacements of the membrane were recorded at every 2 million cycles (see Fig. 6a). As can be seen from Fig. 6b, the overall displacement and the switch-off (release) time of the switch did not change noticeably.

A micrograph and a scanning electron microscope (SEM) image of the fabricated RF-MEMS SPDT switch are given in Fig. 7. The performance parameters of the RF-MEMS SPDT switch are given in Fig. 8. The fabricated SPDTs have an insertion loss of about 2 dB and an isolation of about 15 dB at the operational frequency of 30 GHz.

V. Thermal Management

Apart from RF aspects, thermal issues were also taken into account during the design process of the highly-integrated module architecture. In order to retain the scalability and flexibility of the proposed antenna system, a heat removal concept has been developed conducting the dissipated power towards heat sink perpendicular to multilayer module board (see Fig. 9a). For this purpose the multilayer PCB provides not only cavities for the MMICs but also gridded grooves milled down to the ground plane (L3) which likewise serves as a first heat spreader. During the assembly process, a metal grid is partially embedded into these grooves and joined with the multilayer board using a thin layer of thermally conductive adhesive (G1). To maximize the available area for the planar circuits on the bottom layer (L1), openings are provided in the metal grid. Since the proposed cooling structure has very short heat paths to an external heat sink via the metal grid, the ground layer (L3) can be chosen sufficiently thin to be in line with conventional PCB technologies. The simulated temperature difference between the junction of the MMIC and the heat sink remains constant at 17 K assuming a heat emission of 1.2 W per chip. Fig.9b illustrates the corresponding temperature distribution for a module board with 144 MMICs. Due to the heat conduction vertical to the multilayer PCB, the variation of the module size does not have any appreciable influence on the temperature gradient.

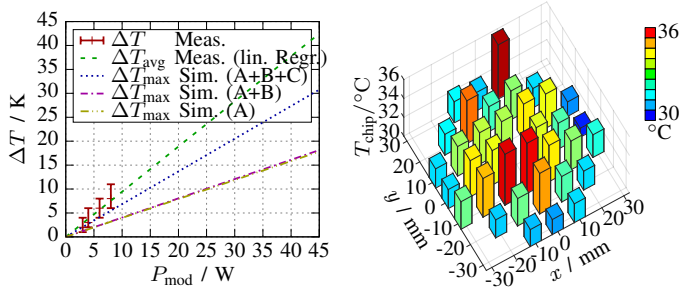
The heat removal concept has been verified by thermal stationary measurements using a module board consisting of 36 chips. For different power dissipation levels P_{mod}, the measured temperature gradient ΔT between the individual MMICs and the metal plate is shown in Fig. 10a. Since the



(a) Perspective view of a submodule; Hole in the metal plate is applied only in the measurement setup to obtain the chip temperatures by an IR camera. (b) Temperature distribution on a module board with 144 MMICs

Fig. 9. Thermal stationary simulation model of the scalable cooling concept.

available MMICs generate only a limited amount of heat, the average temperature increase was estimated by linear regression to be 40.7 K for the maximum intended power dissipation of 1.2 W per chip. The thermal measurements show good agreement with the simulation results of model (C) in which the contact surfaces between the metal grid and plate have additionally been substituted by a homogeneous thermal contact resistance [9]. The measured temperature distribution over all 36 MMICs of the module board while applying a heat emission of P_{mod}=8.46 W is illustrated in Fig. 10b.



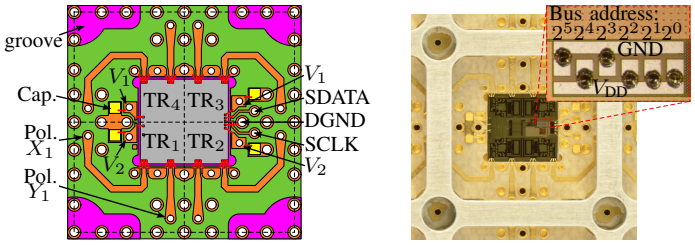
(a) Temperature gradient

(b) Measured temperature distribution while applying an heat emission of P_{mod}=8.46 W

Fig. 10. Thermal stationary measurement and simulation results of a module board with 36 chips. Simulation models taken into account: (A) ideal, (B) Holes in the metal plate, (C) Thermal contact resistance between the metal grid and plate [9].

VI. Assembly and Packaging

The module architecture is partitioned into identical subgroups of 2×2 transceivers. Fig. 11 shows the detailed arrangement of all structures which are situated on the component side of a single submodule. As can clearly be seen, the available area is utilized optimally by the rotation-symmetric configuration of the 4 dual-polarized antenna elements. Since the 4 transceivers on the MMIC are fully controlled via a digital I²C bus interface, two wires – SCL (clock) and SDATA (bi-directional data) – are required for communication. A unique bus address for each MMIC is set by intra-chip wire-bonded jumpers. Besides that, only two wires for DC supply (3.3 V/2.5 V) must be provided.



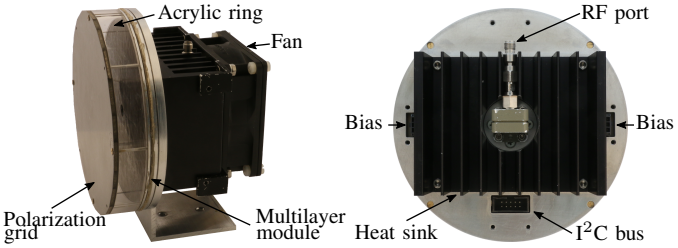
(a) Layout without metal grid

(b) Photograph with metal grid

Fig. 11. Assembled submodule of the active phased array transceiver.

VII. Active Reflectarray Antenna

After the successful evaluation of all required components, a complete phased array transceiver with 144 radiating elements has been realized (see Fig. 12). Subsequently, the calibration of the active reflectarray antenna has been conducted in the near field according to the proposed method in [2]. Once the phased array antenna has fully been calibrated, the amplitude and phase values of the individual channels can be precisely adjusted to synthesize the intended radiation pattern.



(a) Perspective view

(b) Back side without cooling fan

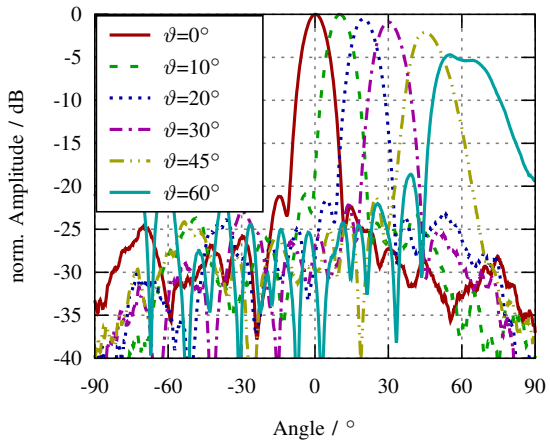
Fig. 12. Active folded reflectarray transceiver with fully monolithically integrated RF-MEMS SPDT switches.

Comprehensive far field measurements have been carried out in both TX and RX mode for various scanning angles in the E- and H-plane. However, since the far field characteristics are very similar for both communication directions, the radiation patterns of the active reflectarray transceiver is shown for TX mode only. The measured radiation diagrams at 30 GHz for different scan angles in the E- and H-plane are presented in Fig. 13. The 3 dB-beamwidths for boresight radiation are 9.4° and 10.1° in the E- and H-plane, respectively. In accordance with the reduced effective aperture for larger elevation angles, a broadening of the mean beam is observed in both planes.

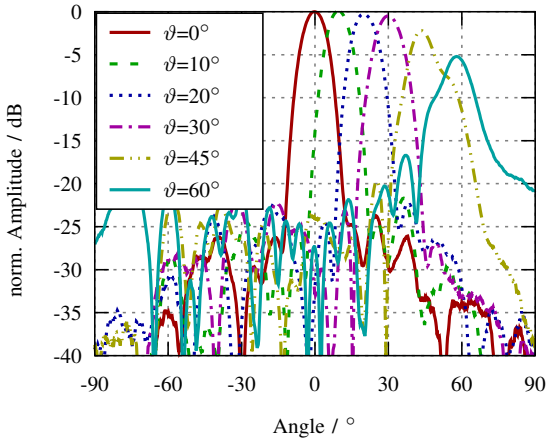
Finally, the measured gain of the active reflectarray transceiver in TX mode at different scan angles in the E- and H-plane is shown in Fig. 14. Independent of the scan angle, an increase in gain is observed for higher frequencies. This trend can be basically explained by the frequency response of the MMICs. In the intended operational band from 29.5 GHz to 31 GHz a maximum gain of 26.2 dB is obtained.

VIII. Conclusion

A highly-integrated phased array transceiver equipped with fully monolithically integrated RF-MEMS SPDT switches has been presented for the first time. The module architecture is

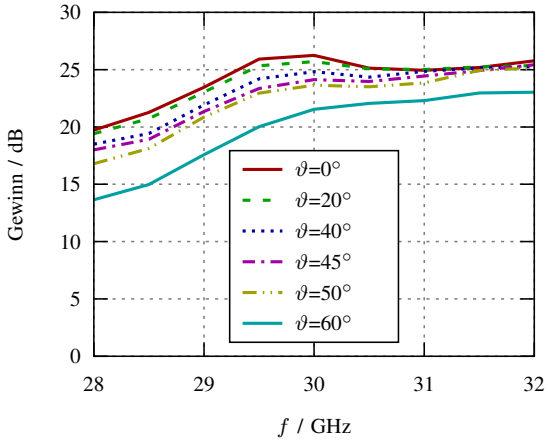


(a) E-plane

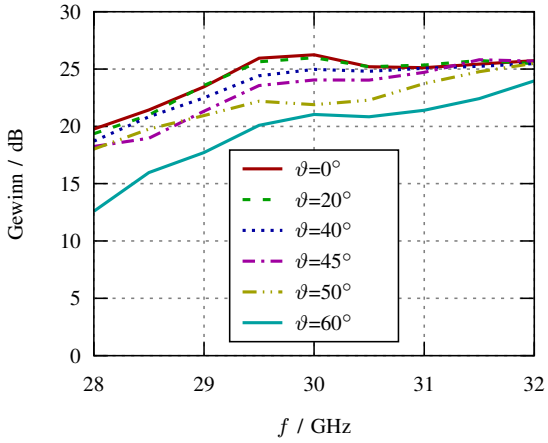


(b) H-plane

Fig. 13. Measured radiation diagrams of the active reflectarray antenna at 30 GHz for different scan angles in the H-plane.



(a) E-plane scan



(b) H-plane scan

Fig. 14. Measured gain of the active reflectarray antenna in TX mode at different scan angles in the E- and H-plane.

based on a 3D multilayer PCB design with the emphasis on a scalable and affordable solution. The complex transceiver chipset realized in a 0.25 µm SiGe BiCMOS technology is particularly suitable for this purpose due to the inherent analog and digital integration. In addition, RF-MEMS SPDTs have been fully monolithically integrated into the SoC to tackle the lack of low-loss millimeter-wave switches. Robustness and reliability tests of employed RF-MEMS components shows excellent results. Finally, their practical applicability has successfully been demonstrated by numerous far field measurements of a 144-element phased array transceiver.

Acknowledgment

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