1 Introduction

For information transfer and processing often signals are required with fixed frequency (for example as a carrier for modulation). These signals are generated according to the requirements and frequency range either by simple $R$-$C$-generators, $L$-$C$, or quartz oscillators or by complex frequency synthesis circuits. In this lab you will learn the design, operation, and parameters of oscillators and PLL frequency-synthesis-circuits.

Most of the modulation schemes used today (e.g. QAM, PSK, etc.) transcode information by changing the amplitude and/or phase of a carrier signal. To conserve power and minimize interference of other receivers, the carrier is often suppressed, which means that there is no spectral carrier power in the modulated signal. Because already minute deviations of the carrier’s phase can lead to demodulation errors, it is necessary to provide the demodulator at the receiver with a coherent carrier that matches with the original carrier in phase and frequency. Only by doing this, a correct retrieval of the phase information can be assured. To achieve this, synchronization circuits are used, based upon the principle of a phase locked loop.

2 Oscillators

Circuits for generating oscillations can be divided into two types:

1) **Double-pole oscillators**
   - produce oscillations by de-damping of an oscillating circuit by using components with a negative differential resistance (i.e. Gunn oscillators),

2) **Quadrupole oscillators**
   - produce oscillations by using the in-phase feedback of an amplifier.

In the following we deal with quadrupole oscillators only.

2.1 The Conditions for Oscillation

2.1.1 Quadrupole with Feedback Network

A quadrupole oscillator consists of an active (amplifier) quadrupole and a feedback network (Fig. 1).

This quadrupole with feedback is characterized as below:

\[
U_1 = U_3 + U'_1, \quad (1)
\]

\[
U_2 = v U_1, \quad (2)
\]

\[
U_3 = k U_2 = k v U_1. \quad (3)
\]
$U_{1,2,3}$ are arbitrary system parameters (voltage, power, etc.) in complex notation. The input is $U'_1$, the gains of the amplifier or quadrupole with feedback are $v$ or $k$.

An oscillator is supposed to oscillate without external signals, i.e. $U'_1 = 0$. Consequently the result from (3) is

$$U_3 = kvU_1 = U_1.$$ (4)

From this the general oscillation condition can be derived:

$$kv = 1.$$ (5)

This can be split up into an amplitude condition

$$|k||v| = 1$$ (6)

and a phase condition

$$\varphi_k + \varphi_v = 2n\pi, \quad n \text{ integral}$$

with

$$\varphi_k = \arg\{k\}, \quad \varphi_v = \arg\{v\}$$ (7)

This is called the Barkhausen stability criterion. If the feedback network or the amplifier is frequency selective, the oscillation condition is fulfilled only for certain frequency intervals, ideally at only one discrete frequency $f_0$. However, resulting from the finite quality of the circuit components, frequencies with $f \approx f_0$ meet this condition as well; a finitely narrow spectrum arises. The closed loop gain $v'$ becomes infinite with fulfilled oscillation condition:

$$\lim_{k\nu \to 1} v' = \lim_{k\nu \to 1} \frac{v}{1 - k\nu} \to \infty.$$ (8)

Consequently, even minimal input voltages (noise, switch-on impact) produce oscillating, and the amplitude of the oscillator would increase infinitely. Real amplifiers, however, are always non-linear. Their amplification depends on the input amplitude, and usually drops off sharply at the limit of the range of modulation. As the amplitude condition is only fulfilled at an amplification of $|v|$ and this is only given at a certain input amplitude, the output-amplitude of the oscillator is constant – the amplitude is controlled by the non-linearities. These non-linearities produce harmonic oscillations in the output. In real circuits the condition $k\nu = 1$ can not be met exactly, as both $k$ and $\nu$ depend on their circuit environment, the tolerances, and the age of the components. In order to guarantee stable oscillating

$$|k||v| > 1$$ (9)
is chosen, i.e. the feedback is greater than necessary to sustain the oscillation. The oscillation
amplitude is again controlled by the non-linearities of the amplifier, which, however, is now
operated with more power, before its gain fulfills the amplitude condition.

The greater $|k| |v|$ is chosen, the more stable are the oscillations, but the greater is also the
amplitude of the harmonics, because the non-linear part of the gain will increase. Oscillators,
for which a high spectral purity is essential, are therefore provided with an amplitude control.
It controls the gain in a way that the amplification is adjusted to the output: Small output
amplitude (oscillator has not started or oscillation stops) goes along with greater amplification;
great output amplitude (stable oscillations, harmonics shall be reduced) goes along with less
amplification; therefore the amplifier is kept running just at the limit of its range of modulation
which is assumed to be linear.

2.2 Parameters of Oscillators

2.2.1 Higher Order Harmonics

Due to non-linearities of the active elements and the finite selectivity of the frequency deter-
mining elements, there are harmonic distortions of the output voltage of the oscillator. These
are caused by higher order harmonics produced by non-linear behavior (Fig. 2).

These distortions are characterized by the distortion factor

$$k = \sqrt{\frac{\text{effective value of the harmonics}}{\text{total effective value}}} = \sqrt{\sum_{n=2}^{\infty} \frac{U_{n,\text{eff}}^2}{\sum_{m=1}^{\infty} U_{m,\text{eff}}^2}} = \sqrt{\sum_{n=2}^{\infty} \frac{P_n}{\sum_{m=1}^{\infty} P_m}}. \quad (10)$$

As the effective value of the harmonics is generally difficult to measure, the distortion factors
of $n^{th}$ order are defined:

$$k_n = \sqrt{\frac{U_{n,\text{eff}}^2}{\sum_{m=1}^{\infty} U_{m,\text{eff}}^2}} = \sqrt{\frac{P_n}{\sum_{m=1}^{\infty} P_m}}. \quad (11)$$
Another measure of the non-linear distortions is the suppression of the harmonic of \( n \)th order:

\[
a_{nc} = 20 \log_{10} \frac{U_n}{U_1} \text{dBc} = 10 \log_{10} \frac{P_n}{P_1} \text{dBc},
\]

\( \text{dBc} \ldots \text{dB} \) related to the carrier.

### 2.3 Phase Noise – Stability of Frequency

Due to finite quality factors and tolerances of the frequency-selecting elements the oscillation condition of an oscillator is fulfilled not just for a discrete frequency but for a band of frequencies (Fig. 3).

\[u(t) = \hat{u} \left(1 + u_N(t)\right) \cos(2\pi f_0 t + \varphi_N(t)).\]  

(13)

The term \( u_N(t) \) describes the amplitude noise and the term \( \varphi_N(t) \) describes the phase noise (=phase-jitter) (Fig. 4).
Due to the superposed signal the zero-axis crossings of the total signal are shifted and phase jitter emerges. As phase and frequency are differentially connected:

\[ \omega(t) = \frac{d \varphi(t)}{dt}, \]  

the phase jitter determines the instantaneous frequency and consequently the short-term stability of the oscillator. The long-time stability, however, depends on factors like aging and environmental conditions.

For further considerations the amplitude noise is neglected:

\[ u(t) = \hat{u} \cos \left( 2\pi f_0 t + \varphi_N(t) \right). \]  

With the addition theorem

\[ \cos(\alpha \pm \beta) = \cos \alpha \cos \beta \mp \sin \alpha \sin \beta \]  

and the approximation for small angles \((\alpha \ll 1 \text{ rad})\)

\[ \cos \alpha \approx 1, \quad \sin \alpha \approx \alpha, \]  

it is with (15)

\[ u(t) \approx \hat{u} \cos(2\pi f_0 t) - \hat{u} \varphi_N(t) \sin(2\pi f_0 t), \]  

\[ u(t) \approx u_{\text{osc}}(t) + u_{\varphi}(t). \]  

With these approximate calculations the carrier power of a resistance \(R\) can be written as

\[ P_{\text{osc}} = \frac{\hat{u}_{\text{osc}}^2}{2R} = \frac{\hat{u}^2}{2R}. \]  

and the phase-noise power as

\[ P_\varphi = \frac{\hat{u}_\varphi^2}{2R} = \frac{\hat{u}_\varphi^2 \varphi_N^2(t)}{2R}. \]  

The ratio of (measured) phase-noise power and carrier power is a measure for the phase jitter:

\[ \frac{P_\varphi}{P_{\text{osc}}} = \frac{\hat{u}_\varphi^2 \varphi_N^2(t)}{\hat{u}^2} = \varphi_N^2(t). \]  

From the relation

\[ \Delta \varphi = \frac{\Delta \omega}{\omega} = \frac{\Delta f}{f}, \]  

it results as a measure for the short-term stability of the oscillator

\[ \frac{\Delta f}{f} = \sqrt{\varphi_N^2(t)} = \sqrt{\frac{P_\varphi}{P_{\text{osc}}}}. \]
As the oscillator signal shows not only the phase jitter but also the amplitude noise and as with this experiment only the total noise power can be measured, the latter must still be corrected [2]:

\[ P_\phi = \frac{P_N}{2}. \]  

(25)

You get the total noise power \( P_N \) by integrating the noise-power density \( \Psi(f) \):

\[ P_N = \int_0^\infty \Psi(f) \, df. \]  

(26)

The relation between the measured curve \( P(f) \) and the distribution of the noise-power-density \( \Psi(f) \) is given by

\[ \Psi(f) = \frac{P(f)}{f_{BW}} \]  

(27)

and \( f_{BW} \) as the measure bandwidth of the spectrum analyzer.

Another parameter frequently used for describing the spectral purity is the **SSB phase noise density** (Single-Sideband of the phase noise density), which is defined as ratio between the power in one hertz bandwidth at frequency distance of \( f_m \) from the carrier to the total power of the carrier and which is noted:

\[ \Psi_{SSB}(f_m) = 10 \log \left( \frac{1}{P_{osc}(f_0)} \int_{f_0 + f_m - 0.5 \text{Hz}}^{f_0 + f_m + 0.5 \text{Hz}} \Psi(f) \, df \right) \text{dBc/Hz}. \]  

(28)

Practically, this quantity can be approximated by the ratio of the power measured by a spectrum analyzer at a distance of \( f_m \) to the carrier and the power at the carrier frequency:

\[ \Psi_{SSB}(f_m) \approx 10 \log \left( \frac{P_{SSB}(f_0 - f_m)/f_{BW}}{P_{osc}(f_0)} \right) \text{dBc/Hz}. \]  

(29)

### 2.4 Phase Noise – Measurements

This section gives an overview of the operating principle of different phase noise measurement methods. Additional methods as well as a deeper examination can be found at [3].

**Direct Spectrum Measurement** The output signal of the oscillation source under test (SUT), is fed into a spectrum analyzer where the spectral power density is measured. The accuracy of this method is limited by the dynamic range, the resolution, as well as the phase noise of the analyzer’s local oscillator.

**Heterodyne Measurement** Here, the signal is downconverted into the baseband. A high resolution frequency counter measures the frequency repeatedly in a definable time gate of duration \( \Delta t \). From the different measured frequencies \( y \) during the duration \( \Delta t \), the so-called Allan variance \( \sigma_y(\Delta t) \) and the resulting spectral power density can be calculated. This method can be used for measuring the phase noise at an offset between 100 Hz and 10 kHz relative to the carrier [3].
**Measurement with a phase detector, quadrature method** The measurement setup according to Fig. 5 consists of a reference source, a mixer, a low pass filter and a low noise amplifier (LNA). At the mixer inputs, the signals of SUT and reference source are present. If both sources have the same frequency, the resulting summed part $2f_0$ will be filtered out by the low pass filter, whereas the difference signal prevails. If the signals of the sources are phase shifted by $90^\circ$ (they are in quadrature to each other), this results in a difference signal with a DC offset of 0 V. Superimposed frequencies are linear to the phase error between SUT and reference source and get amplified by the LNA. The resulting spectrum can be measured with a spectrum analyzer. To make it clear: The mixer acts as a phase detector, if both sources’ signals are in quadrature. To ensure quadrature, one of the sources (usually the reference source) has to be tunable and there has to be a feedback network between the output of the low pass filtered mixer signal (the phase detector) and the tunable oscillator. This creates a so-called phase locked loop (PLL, see Chapter 3) [3]. A prerequisite for this method is a reference source with low phase noise, because this limits the accuracy of the measurement. If the phase noise is to be measured at frequency offsets smaller than the bandwidth of the low pass filter, a more complex system is needed, because otherwise measurements will yield lower results than actually present [3].

![Circuit diagram for phase detector method](image-url)

Fig. 5: Circuit diagram for phase detector method [3].
3 Phase Locked Loop (PLL) and Frequency Synthesis

A phase locked loop, furthermore denoted as PLL, is a closed-loop control to create a fixed phase relation between the output signal of a VCO and a reference signal. PLLs are used for clock and carrier recovery (e.g. for the color carrier signal in color TV), for frequency and phase modulation, as well as demodulation and clock generation/frequency synthesis, amongst other things. Figure 6 shows the schematics of a PLL. It consists of a reference oscillator XO, a phase detector PD with a phase detector frequency $f_{PD}$, a loop filter LF, a voltage controlled oscillator VCO, and two dividers $M$ and $N$ [5].

![ PLL Schematic Diagram ]

**Fig. 6: Schematic of a PLL.**

Due to their high frequency stability, quartz oscillators are often used as reference source. Its frequency is $f_{XO}$ and is – due to the limited frequency range of quartz oscillators – usually smaller than 200 MHz [5]. At the phase detector input, the reference frequency divided by $M$ and – over the feedback network – the output frequency of the VCO $f_o$ divided by $N$ is present. This results in the phase detector frequency

$$f_{PD} = \frac{f_o}{N} = \frac{f_{XO}}{M}.$$  

(30)

Depending on the actual implementation (see Chapter 3.1.1) at the phase detector output now occur voltage or current pulses $u_d$ proportional to the phase difference of the two signals. The low pass loop filter converts these pulses into a slowly changing tuning voltage $u_{tune}$, which can be fed into the VCO. This changes the phase of the VCOs output single in such a way that the two input signals at the phase detector are forced in phase. This is called the locked state of the PLL. There is now a direct relationship between reference frequency and output frequency of the PLL [5]:

$$f_o = N \cdot \frac{M}{M} f_{XO}.$$  

(31)

This allows to bind the frequency as well as the stability of a VCO in the GHz range to the one of a highly stable reference oscillator in the low MHz range. This lowers the phase noise of the VCO significantly [5].

### 3.1 Components of a PLL

Here the most prominent components of a phase locked loop shall be introduced and their functioning principle explained.
3.1.1 Phase Frequency Detector (PFD)

Figure 7 shows the general schematic of a PFD. It consists of two D flip flops (D-FF) as well as a NAND gate. The inputs $D$ are constantly kept on “1” (logical high). To explain the principle of function, we assume that frequency $f_1$ is higher than $f_2$. With a rising edge of $f_1$ FF1 gets set. Only if a rising edge of $f_2$ is present at the input of FF2, $Q_2$ jumps shortly to “1” and both flip flops get reset via the NAND gate. This leads to a “0” (logical low) at $Q_{1/2}$ (see [4]). $U_1$ is therefore longer active than $U_2$. The same is true for $U_2$, if $f_2 > f_1$.

For the case of $f_1 = f_2$ with a phase difference between the two signals (i.e. the rising edge of $f_2$ comes after that of $f_1$), $U_1$ is also longer active than $U_2$. This also leads to the PDF having no residual phase error $\phi_e(t)$, because it gets reduced to 0 (see [4]).

![Fig. 7: Schematic of a PFD.](image)

PDFs are build almost exclusively in connection with a charge pump, that converts the PFDs output voltage, which is proportional to the phase difference, into current pulses, used to correct the phase error. The PFD’s output voltages $U_1$ and $U_2$ are switching the current sources as shown in Fig. 8a, which leads to positive and negative current pulses. Averaged over one period and for phase errors between

$$-2\pi < |\phi_e| < 2\pi$$

the output current of the charge pump, caused by the phase difference $\phi_e$, multiplied by the charge pump gain $K_d=I_{CP}$ is ([5])

$$\bar{i}_{CP} = \frac{K_d}{2\pi} \phi_e$$

(32)

and follows a saw tooth profile (see Fig. 8b). Figure 8c exemplary shows the output of the charger pump in the case of $f_1 = f_2$ with an constant phase error.
3.1.2 Voltage Controlled Oscillator (VCO)

The basic criteria for oscillation was already covered in Chapter 2. To change the output frequency, the resonator gets tuned. For LC resonators after [1] this is generally done with capacitive diodes, whose capacities can be tuned with a DC voltage \( u_{\text{tune}} \). The resulting circuit is pictured in Fig. 9 with inductance \( L \), capacitive diodes \( C_{1/2} \), and resistance \( R_P \), which represents the loss of inductance and capacitance.

The resonance frequency is calculated as

\[
\omega_R = 2\pi f_R = \frac{1}{\sqrt{L C_{\text{eq}}}} \quad \text{with} \quad C_{\text{eq}} = \frac{1}{C_1} + \frac{1}{C_2}.
\]  

Most important for low phase noise and a stable output frequency are the quality of the resonating structure (unloaded quality), which for a parallel resonator is

\[
Q = R_P \sqrt{\frac{C_{\text{eq}}}{L}}.
\]
If no tuning voltage is present, the oscillator produces the free running angular frequency $\omega_c$. If a tuning voltage is applied, the frequency changes by the oscillator gain $K_o$, $[K_o]=\text{MHz/V}$. Then there exists a connection between tuning voltage $u_{\text{tune}}$ and output phase of the VCO after [4] of

$$\dot{\Psi}_o(t) = \frac{d}{dt} (\omega_o t + \phi_o(t)) = \omega_c + K_o u_{\text{tune}}(t).$$  \hfill (35)

### 3.1.3 Frequency Divider

The transfer function of a frequency divider for the input frequency $f_{\text{in}}$, the output frequency $f_{\text{out}}$, and the factor $N$ is

$$f_{\text{out}} = \frac{1}{N} f_{\text{in}}.$$  \hfill (36)

According to [6], a frequency division by $N$ reduces the spectral power density of phase noise by $20\log N \text{dB}$. However, in the closed loop transfer function (54) in chapter 3.3 the factor $F_M(s) = \frac{1}{N}$ appears in the feedback loop as multiplier (see Fig. 10). This means that the phase noise worsens by $20\log N \text{dB}$. For a factor of 100 for example the phase noise would be raised by 40 dB. Therefore, this factor should be kept as low as possible.

Digital frequency dividers are usually built from D- or JK-flip flops [5]. For price and power consumption CMOS technology is preferred. The flip flops get chained together to form binary and partly programmable synchronous counter (with reset logic). In the following, the counter will be denoted by $B$ and its set division factor by $b$. For high frequencies, prescalers – available for frequencies higher than 6 GHz – are used.

**Single modulus prescaler**  A divider with a fixed division factor $\frac{1}{P}$, realized for example in GaAs or SiGe technology, is added in the feedback network. A disadvantage is that now the whole factor $N$ is always an integer multiple $b$ of $P$:

$$N = bP.$$  \hfill (37)

**Dual modulus prescaler**  To avoid the disadvantage of the single modulus prescaler, dual modulus prescalers are used. These are realized in the form of $\frac{P}{P+1}$ and are build from a prescaler $\frac{1}{P}$, and a pulse swallow function, which swallows one clock pulse. This is realized by using an additional counter $A$ with its starting value $a$. Starting with the pulse swallow function activated (prescaler value corresponds to $\frac{1}{P+1}$), both counters $A$
and $B$ are counted down. When $A$ has reached zero (after $a(P + 1)$ steps), the pulse swallow function is deactivated. Now the prescaler value corresponds to $\frac{1}{P}$, while $B$ is counted down to 0 for $(b - a)P$ clock cycles. This leads to a factor of:

$$N = Pb + a \quad \text{with} \quad b = \left\lfloor \frac{N}{P} \right\rfloor \quad \text{and} \quad a = N \mod P.$$

$N$ is limited by the condition $b \geq a$.

To not just achieve integer factors, **fractional-n-architectures** are used. According to [6] the accumulator switches between two or more values for $N$ in such a way, that the average factor is the desired fraction $N_{\text{frac}}$. For example, if we switch between the two values $N$ and $N+1$, according to [6] this results in

$$N_{\text{frac}} = N + \frac{K}{F}.$$  

Where $K$ is the number of clock cycles, during which the system divides by $N+1$ and $F$ is the overall number of clock cycles, over which an averaged division factor $N_{\text{frac}}$ occurs. The switching produces spurious signals which can be minimized by compensation circuits. Further information and a deeper explanation of the accumulator and these compensation circuits can be found in [6].

### 3.2 Integer-N-PLL and Fractional-N-PLL

**Integer-N-PLL** This type of PLL works like explained in the beginning of this chapter (see Fig. 6). In the feedback loop there is an integer divider, which can be implemented with or without single-, dual-, or even quad-modulus-prescaler. The minimal frequency resolution, which dictates the minimal output frequency change possible, is equal to the phase detector frequency $f_{PD}$, which is dependent on the $N$ divider in the feedback loop:

$$f_{PD} = \frac{f_o}{N}.$$  

In [6] there is an example for a mobile network application, which describes the problems that can arise in regards to frequency resolution and the impact of a high division factor on the phase noise: If a high output frequency (e.g. $f_o$=960 MHz) relative to the frequency resolution (e.g. $f_{PD}$=30 kHz) is desired, a division factor of 32 000 is needed. This leads to a worsening of the phase noise of about 90 dB. With an integer-N-PLL, there will always be a trade-off to be made between frequency resolution and tolerable phase noise. This can be avoided by using a fractional-N-PLL.

**Fractional-N-PLL** The goal is to achieve a smaller division faction $N$ and a higher phase detection frequency $f_{PD}$. For this, the fractional-N-PLL must achieve a fraction of the phase detection frequency as frequency resolution. This is possible due to the fractional-N architecture as described in chapter 3.1.3. Thanks to the higher phase detection frequency and thus the lower division factors, the phase noise gets reduced, compared to the integer-N-PLL. Additionally, a wider loop filter bandwidth can be used, which leads to faster locking of the PLL. The aforementioned example can now be used for a fractional-N-PLL. To achieve a frequency resolution of 30 kHz at 960 MHz output frequency, a fractional resolution of 16 is sufficient ([16]).
to lower the phase noise already by about 24 dB, because the division factor is 2000 instead of 32000. In this case, 15 clocks will be divided by 2000 whereas 1 clock gets divided by 2001. According to (39) it is $K=1$ and $F=16$. Spurious signals are created for

$$f_{PD} \quad \text{and} \quad \frac{f_{PD}}{F}$$

and its harmonics, according to [6]. These spurious signals can be reduced by around 40 dBc by using compensation circuits. For additional suppression, loop filters of 3rd or 4th order are necessary (see Chapter 3.4).

### 3.3 Description in the Frequency Domain

In this section, a linear connection between the input and the output phase of the PLL shown in Fig. 6 is derived. For this, the input signals of the phase detector are assumed to be sinusoidal.

$$u_i(t) = \hat{u}_i \sin (\omega_i t + \phi_i) = \hat{u}_i \sin (\Psi_i(t)),$$  \hspace{1cm} (42)

$$u_r(t) = \hat{u}_r \cos (\omega_r t + \phi_r) = \hat{u}_r \cos (\Psi_r(t)).$$  \hspace{1cm} (43)

For the phase detector, a PDF with CP is used. Therefore, the tuning voltage $u_{tune}$ after the loop filter with the transfer function $f(t)$ according to [4] is

$$u_{tune}(t) = K_d \Psi_e(t) \quad \text{with} \quad \Psi_e(t) = \Psi_i(t) - \Psi_r(t).$$  \hspace{1cm} (44)

Assuming equal input frequencies

$$\omega_i = \omega_r \Rightarrow \Psi_e(t) = \phi_i(t) - \phi_r(t) = \phi_e(t),$$  \hspace{1cm} (45)

the tuning voltage is derived to

$$u_{tune}(t) = u_{tune,0} + K_d \phi_e(t),$$  \hspace{1cm} (46)

where $u_{tune,0}$ is a DC voltage that allows for $\omega_i=\omega_r$. With the tuning voltage from (46) and (35) for the output signal of the VCO, it follows according to [4]

$$\omega_o + \dot{\phi}_o(t) = \omega_c + K_o u_{tune,0} + K_o K_d \sin (\phi_e(t)).$$  \hspace{1cm} (47)

The relation between the VCO’s output frequency and $\omega_r$ is given over a factor with the transfer function $f_M(t)$ in the feedback loop as

$$\omega_o \frac{1}{f_M(t)} = \omega_r N = \omega_o = \omega_c + K_o u_{tune,0}.$$  \hspace{1cm} (48)

For the phase it follows

$$\dot{\phi}_o(t) = K_o K_d \sin (\phi_e(t)).$$  \hspace{1cm} (49)

With the Laplace transform of (49) and the assumption $\phi_o(0)=0$ follows

$$s\Phi_o(s) = K_o K_d \Phi_e(s).$$  \hspace{1cm} (50)
3 Phase Locked Loop (PLL) and Frequency Synthesis

\[ \Phi_o(s) = \frac{K_oK_d}{s} \Phi_e(s). \tag{51} \]

For the frequency range the schematic depicted in Fig. 10 can therefore be used. The regulation loop is closed by the feedback via the frequency divider \( F_M(s) \) (see (48)). From this, it directly follows

\[ \Psi_R(s) = F_M(s)\Psi_o(s). \tag{52} \]

The relation between the input and the output phase is therefore

\[ \Phi_i(s) - \Phi_o(s)F_M(s) \frac{K_dK_oF(s)}{s} = \Phi_o(s). \tag{53} \]

Rearranged and using \( K = K_oK_d \) the transfer function of the closed loop (closed-loop gain) of the PLL can be derived:

\[ H(s) = \frac{\Phi_o(s)}{\Phi_i(s)} = \frac{KF(s)}{1 + KF(s)F_M(s)} = \frac{G(s)}{1 + G(s)F_M(s)} \tag{54} \]

with the open loop gain

\[ G(s) = \frac{KF(s)}{s}. \tag{55} \]

Furthermore, the following relationship between the phase difference at the phase detector and the input phase exists:

\[ \Phi_e(s) = \Phi_i(s) \frac{1}{1 + G(s)}. \tag{56} \]

### 3.4 Loop Filter

In this section, the design of a loop filter is described. For this, the structure, the filter order, the desired phase margin, the bandwidth of the filter, and the matching pole ratio is given. Figure 11 shows a passive loop filter for charge-pump-PFDs. If the output voltage of the charge pump is not high enough for the tuning range of the VCO, active filters have to be used, as described in Section 3.4.2. Because active components produce additional phase noise, higher costs, and an overall higher complexity of the circuit, passive filters should be used, where possible.

First, the question of the filter order shall be discussed. A order of 2 or higher is necessary, if unwanted signals from the reference or other spurious signals outside of the loop filter

![Diagram of PLL](image)

**Fig. 10:** PLL in frequency range for locked state.
bandwidth need to be suppressed. For the **phase margin** are according to [5] values in the range of 40° to 55° typical. The phase margin has a big influence on the lock time and stability of the PLL. According to [5] a phase margin of 48° is the optimal value for lock times and 50° is a good start value for minimal RMS phase errors.

The biggest influence though has the **loop filter bandwidth**. Too wide, and spurious signals are not filtered out. Too narrow, and the PLL lock time is too long. Therefore, the loop filter bandwidth is always a trade-off between lock time and spurious suppression. According to [5], the loop filter bandwidth has to be chosen narrower than $\frac{f_{PD}}{2\pi}$ to assure stability. Additionally, the capacities of the filter have to taken into account. The capacity nearest to the VCO should be at least three times as big as the input capacitance of the VCO, which changes with the output frequency and thus can have a negative, non-foreseeable influence on the transfer function of the filter.

For filters of 3rd and 4th order the **pole ratio** $(T_{31}$ and $T_{43})$ can be used to determine the position of the pole relative to the poles $T_1$. For passive filters values in the range of 0 to 1 for active filters values larger than 1 can be used. According to [5], the loop filter impedance $F(s)$ can be denoted as a function of poles $T_1$, $T_3=T_{31}T_1$ and $T_4=T_{31}T_{43}$, the root $T_2$, as well as the overall capacitance $A_0$ of the loop filter as

$$F(s) = \frac{1 + sT_2}{A_0s(1 + sT_1)(1 + sT_{31}T_1)(1 + sT_{31}T_{43})}.$$  \hspace{1cm} (57)

Given the phase margin $\phi$ and the corner frequency $\omega_c$, the time constants $T_1$ and $T_2$ can be calculated. The first equation needed for this is that of the open loop gain (55). Calculated for the corner frequency and added to 180°, the phase margin follows as [5]

$$\phi = 180^\circ + \arctan(\omega_cT_2) - \arctan(\omega_cT_1) - \arctan(\omega_cT_{31}T_1) - \arctan(\omega_cT_{31}T_{43}).$$  \hspace{1cm} (58)

The second equation can be derived according to [5] as the derivation of (58). For $\omega_c$ and set equal to zero, it is

$$\frac{d\phi}{d\omega} \bigg|_{\omega=\omega_c} = 0.$$  \hspace{1cm} (59)

Depending on the filter’s order, the time constants $T_1$ and $T_2$ can be calculated in closed form for 2nd order or numerical for filters of higher order. For further calculations, the “optimization
factor gamma \( \gamma \) is needed. It is deeply connected to the phase margin. As starting value 1.0 is recommended. In this lab only filters of 2\(^{\text{nd}}\) order will be investigated. More on filters of higher order and \( \gamma \) can be found in [5].

### 3.4.1 Filters of 2\(^{\text{nd}}\) Order

Filters of 2\(^{\text{nd}}\) order are loop filters the easiest to design, because they have a closed solution. Additionally, they have the lowest thermal noise and the highest capacitance values near the VCO. For 2\(^{\text{nd}}\) order filters it is \( T_3 = T_4 = T_{31} = T_{43} = 0 \). The transfer function is as follows:

\[
Z(s) = \frac{1 + sC_2R_2}{s(C_1 + C_2)} = \frac{1 + sT_2}{sA_0(1 + sT_1)}. \tag{60}
\]

To calculate the needed component values, (58) is used to derive

\[
\phi = 180^\circ + \arctan(\omega_cT_2) - \arctan(\omega_cT_1) \tag{61}
\]

If it is derived \( \omega \) according to (59) one gets

\[
\left. \frac{d\phi}{d\omega} \right|_{\omega = \omega_c} = 0 = \frac{T_2}{1 + \omega_c^2T_2} - \frac{T_1}{1 + \omega_c^2T_1}. \tag{62}
\]

From this \( T_2 \) can be approximated as

\[
T_2 = \frac{\gamma}{\omega_c^2T_1}. \tag{63}
\]

By substituting (63) in (61) \( T_1 \) can be determined:

\[
T_1 = \frac{\sqrt{(1 + \gamma)^2\tan^2\phi + 4\gamma - (1 + \gamma)\tan\phi}}{2\omega_c}. \tag{64}
\]

The equations above yield the root \( T_2 \) and the pole \( T_1 \). These can be used to calculate all necessary component values:

\[
A_0 = \frac{C_1T_2}{T_1} = \frac{K_dK_o}{N\omega_c^2} \sqrt{\frac{1 + \omega_c^2T_2^2}{1 + \omega_c^2T_1^2}}, \tag{65}
\]

\[
\implies C_1 = A_0 \frac{T_1}{T_2}, \quad C_2 = A_0 - C_1, \quad R_2 = \frac{T_2}{C_2}. \tag{66}
\]

### 3.4.2 Active Filters

Active filters are used if the VCO needs a higher tuning voltage than can be delivered by the charge pump. For this, an operational amplifier (OP) is integrated into the loop filter. The concept and the equations for the time constants from Section 3.4 can be used analogous for active loop filters. However, as will be shown later, calculation of the components is not
analogous. Because the OP introduces additional phase noise, a minimum filter order of 3 is recommended [3]. The additional RC sections of the new filter suppress the influence of the OP noise. For a phase detector with charge pump, there are generally two approaches: the **simple gain approach** and the **standard feedback approach**.

The **Simple-Gain-Approach** used in this lab (see Fig. 12) a non-inverting OP is put between the loop filter of 2nd order and the rest of the RC parts, decoupling them. The gain $A$ is determined by $R_a$ and $R_b$ according to the non-inverting configuration:

$$ A = \frac{R_a + R_b}{R_b} . $$

(67)

Disadvantageous is the fact that the noise of the OP gets multiplied with the gain [5]. This noise is suppressed by the following RC low pass filter.

![charge pump, i_{CP}] C_1 R_2 C_2 R_a R_b + VCO, u_{tune} C_3 R_3 -

Fig. 12: Active filter Simple-Gain-Approach [5].

The **Standard-Feedback-Approach** compensates the disadvantage of the OP noise getting multiplied by the gain. According to [5] the OP is used in inverting configuration instead where a part of the filter structure is implemented into the feedback. This prevents the OP’s noise to get amplified by the gain. To suppress spurious signals, the operating point $u_{OP}$ is set to half of the charge pump supply voltage. The Standard-Feedback-Approach is preferable compared to the Simple-Gain-Approach. But for this, the charge pump needs to be able to change its polarity. Also no gain is possible with the Standard-Feedback-Approach (unity gain). Therefore it is not used in this lab.

For calculating the components there is no difference, apart from the sign of the gain. In the following description, a positive gain and an active filter 3rd order is assumed. The impedance of the active loop filter of 3rd order can be calculated easily compared to the passive one, because of the decoupling by the OP. With the impedance of the 2nd order filter from (60) and the impedance of a $RC$ low pass filter it follows:

$$ F(s) = Z_1(s)A \frac{1}{1 + sC_3R_3} , $$

$$ F(s) = A \frac{1 + sT_2}{sA_0 (1 + sT_1)(1 + sT_3)} , $$

with

$$ A_0 = C_1 + C_2 , $$

(69)

$$ T_1 = \frac{C_1C_2R_2}{A_0} , \quad T_2 = C_2R_2 , \quad T_3 = C_3R_3 . $$

(70)
For a given phase margin, optimization factor, filter bandwidth, pole ratio $T_{31}$, as well as the capacitance $C_3$, one can calculate the time constants $T_1$ and $T_2$, analogous to the passive filter. This, however, cannot be examined further in this lab.

### 3.5 Noise Influence of the Components

This section examines the influence of the single components noise on the PLL. For this the single side band noise power densities depicted in Fig. 13 shall be taken into account.

![Fig. 13: Overview over the examined noise sources of a PLL.](image)

In regard to Fig. 13, additional transfer functions can be formulated for the respective parameters at the output. With these, the contribution of the separate components to the overall noise of the PLL can be determined.

**Reference oscillator** The reference oscillator’s phase noise $L_{\text{ref}}$ attributes to the overall noise via the transfer function of the closed loop (see (54)), and can be calculated as follows:

$$L_{\text{ref}}(f) \Bigr|_{\text{dBc/Hz}} = 10 \log \left( 10^{ \frac{L_{\text{ref}}(f)}{10} \, \text{dBHz} } \left| H(f) \right|^2 \right). \tag{71}$$

**Phase frequency detector (PFD)** For noise examinations of the PFD a two-part phase noise model according to [5] is used. The first part, the base noise, consists of a component specific normalized noise floor $P_{N\text{floor}}$. It depends on the phase detector frequency $f_{PD}$ and the transfer function of the closed loop $H(t)$:

$$L_{P_{N\text{floor}}}(f_{\text{offset}}) \Bigr|_{\text{dBc/Hz}} = P_{N\text{floor}} + 10 \log \left( f_{PD} \right) + 20 \log \left( \left| H(f) \right| \right). \tag{72}$$

The second part takes into account the influence of the $\frac{1}{f}$-noise with the offset frequency $f_{\text{offset}}$ away from the carrier also over a component specific constant normalized PLL $\frac{1}{f}$ noise $P_{N1/f}$ and the dependency from the output frequency of the VCO $f_o$:

$$L_{P_{N1/f}}(f_{\text{offset}}) \Bigr|_{\text{dBc/Hz}} = P_{N1/f} + 20 \log \left( \frac{f_o}{1 \, \text{GHz}} \right) - 10 \log \left( \frac{f_{\text{offset}}}{10 \, \text{kHz}} \right). \tag{73}$$
The component specific values usually are denoted in the data sheet of the used PLL chip. For the single sideband noise power density of the PDF at the output of the PLL follows:

\[
\mathcal{L}_{\text{PFD}}\bigg|_{\text{dBc}} = 10 \log \left( 10 \frac{\varepsilon_{\text{PN}_{\text{max}}}(f_{\text{OD}})}{10} \frac{\text{Hz}}{\text{Hz}} + 10 \frac{\varepsilon_{\text{PN}_{\text{1/f}}}(f_{\text{OD}})}{10} \frac{\text{Hz}}{\text{Hz}} \right).
\]

**VCO** The VCO is taken into account via the transfer function \( H_{\text{VCO}} \):

\[
\mathcal{L}_{\text{VCO}_{\text{out}}}(f)\bigg|_{\text{dBc}} = 10 \log \left( 10 \frac{\varepsilon_{\text{VCO}}(f)}{10} \frac{\text{Hz}}{\text{Hz}} |H_{\text{VCO}}(f)|^2 \right).
\]

**Loop filter** The phase noise caused by the loop filter is modeled as RMS voltage noise which superimposes the tuning voltage of the VCO. Therefore the same transfer function as that one of the VCO can be used:

\[
\mathcal{L}_{\text{LF}_{\text{out}}}(f)\bigg|_{\text{dBc}} = 10 \log \left( 10 \frac{\varepsilon_{\text{LF}}(f)}{10} \frac{\text{Hz}}{\text{Hz}} |H_{\text{VCO}}(f)|^2 \right).
\]

**Total noise** By summing up all the parts the total phase noise at the PLL output can be calculated as follows:

\[
\mathcal{L}_{\text{PLL}}(f)\bigg|_{\text{dBc}} = 10 \log \left( 10 \frac{\varepsilon_{\text{refout}}(f)}{10} \frac{\text{Hz}}{\text{Hz}} + 10 \frac{\varepsilon_{\text{PPD}}(f)}{10} \frac{\text{Hz}}{\text{Hz}} \\
+ 10 \frac{\varepsilon_{\text{LF}_{\text{out}}}(f)}{10} \frac{\text{Hz}}{\text{Hz}} + 10 \frac{\varepsilon_{\text{VCO}_{\text{out}}}(f)}{10} \frac{\text{Hz}}{\text{Hz}} \right).
\]

**Literature**

4 Questions and Problems on the Lab

Problem 1: Consider a PLL with charge pump current $K_d=0.938$ mA and a VCO with oscillator gain $K_{VCO}=1$ GHz V$^{-1}$. A 2nd order low pass filter is used as loop filter. The reference source’s frequency is 100 MHz. The basic structure is pictured in Fig. 6.

a) The phase detector frequency is supposed to be 50 MHz and the output frequency is supposed to be 11 GHz. Calculate the necessary division factors.

b) The loop filter is supposed to have the following characteristics: Corner frequency=100 kHz, phase margin=48° and gamma optimization factor=1. Calculate the necessary poles and zeros ($T_1$, $T_2$), and the component values.

c) Determine the transfer function of the noise components of the reference source ($H_{ref}$), the loop filter ($H_{LF}$), the VCO ($H_{VCO}$), and the divider ($H_{NDiv}$) using the dependencies for the open loop ($G$), the closed loop ($H$), and the transfer function of the frequency divider in the feedback loop ($F_M$).

d) Now use the provided MATLAB script (available on the Homepage of the Institute). Examine the two signal sources with help of the script $d$ _SourceCompare.m. Which of the signals sources is preferable and why? What is the cause for the spurious signals?

e) Complete the script $LoopFilter.m$ with your calculated values and the transfer functions in $Transferfunctions.m$. Run the main script $e$ _PhaseNoiseCalc.m. Determine the dominating part of the output phase noise for every decade with help of the created plots. Do this for both signal sources. For this, comment out the unused source in the script $SelectSource.m$. Print out the results and bring it to the lab with you.

Hints

- The used scripts are compatible with GNU Octave. However, you have to first load the control package by typing in $pkg load control$.
- Tested with:
  - Octave 4.2.0 x64, Matlab 2016a, Windows 8.1
  - Octave 4.0.0 x64, Matlab 2016a, Ubuntu Linux 16.04
5 Measuring Tasks

5.1 Needed equipment

**SMA 100:** Low Phase Noise RF Source, 9 kHz bis 6 GHz

**RTO1044:** Oscilloscope, 4 channel, 4 GHz BW

**FSW26:** Signal/Spectrum Analyzer, 2 Hz bis 26.5 GHz

**Channel Power Supplies:** 6 V and 16 V

**Measurement Laptop:** Software ADF4155

5.2 Measuring Setup

**PLL** The PLL used in this lab is an Inter-N/Fraction-N-PLL-Synthesizer. The frequency range of the feedback loop is 500 MHz to 8000 MHz. The phase detector frequency can be set up to 125 MHz, but will be set to 50 MHz for this lab. The tuning range of the charge pump voltage is around 5 V.

**The VCO board** On the separate VCO board, four different loop filters are located (three passive, one active), which will be examined during the lab. Also there is VCO whose tuning range is 0 V to 13 V. The frequency profile has to be determined during the lab. The voltage amplification of the active filter is $2.6=8.3$ dB. The feedback loop is closed with the $\frac{f_{VCO}}{2}$ output of the oscillator.

Figure 14 shows the measurement setup. The necessary settings for the PLL are depicted in Fig. 15. For this lab, only the section labeled “RF Settings” is of interest.
Fig. 14: Schematic of the measurement setup.

Fig. 15: Screenshot of the PLL control software.
5.3 Tasks

1) Determine the frequency profile of the VCO for $u_{\text{tune}}$ between 0.5 V and 12.5 V in 0.5 V steps. Determine the tunable range of the CP. Use the RTO as well as the FSW.

**Settings of the RTO**

- Preset
  - CH1 $\Rightarrow$ 1 MΩ DC
  - $\Rightarrow$ Vertical Scale 2 V/Div
  - $\Rightarrow$ Offset 5 V

- Cursor
  - $\Rightarrow$ Track waveform

- MEAS
  - $\Rightarrow$ Main Measurement $\Rightarrow$ MEAN
  - $\Rightarrow$ Envelope $\Rightarrow$ Both

**Settings of the FSW**

- Preset
  - Freq $\Rightarrow$ Start $\Rightarrow$ 9.5 GHz
  - $\Rightarrow$ Stop $\Rightarrow$ 14 GHz
  - BW $\Rightarrow$ 100 kHz

- Marker
  - $\Rightarrow$ Mark Config $\Rightarrow$ Search $\Rightarrow$ Auto Max Peak

2) Determine the free-run frequency of the VCO to the precision of 1 kHz and measure the phase noise.
   Which difficulties are eminent?

**Settings of the FSW**

- MKR $\Rightarrow$ Center = Mkr Freq

**Phase Noise Measurement:**

- Mode
  - $\Rightarrow$ Phase Noise
  - $\Rightarrow$ Phase Noise $\Rightarrow$ Control $\Rightarrow$ Absolute Tolerance 100 kHz

**Single Run**

3) Connect the SMA100 with the FSW26. Be careful that the DC-Block is installed at the input of the spectrum analyzer.

   a) Determine the higher harmonics of the 100 MHz reference signal and calculate distortion factor as well as the suppression of the harmonics.

**Settings of the SMA**

- Preset
  - Freq $\Rightarrow$ 100 MHz
  - Level $\Rightarrow$ 0 dBm

**RF ON/OFF**
5 Measuring Tasks

Settings of the FSW

Freq
⇒ Start 0 Hz
⇒ Stop 1 GHz

BW
⇒ 10kHz

MKR Funct.
⇒ Marker Peak List ⇒ adapt Threshold (~88 dBm)

Sweep
⇒ Sweep Config ⇒ Sweep Points 100001

b) Measure the phase noise at 100 MHz and denote the values for every decade.
Are there spurious signals? If so, where are they coming from?

Settings of the FSW

Phase Noise ⇒ Frontend ⇒ Nominal Frequency 100 MHz
⇒ Control ⇒ Absolute Tolerance 1 kHz
⇒ Freq ⇒ Start 100 Hz
⇒ Stop 1 GHz

4) Build up the PLL with the loop filter of 2nd order and stabilize the VCO to 11 GHz.

a) Is the PLL running in integer- or fractional-N-mode?
   Calculate the necessary division factors.

b) Open the Software ADF4155 and set up everything according to Fig. 15. Change
   the frequency of the reference oscillator in respect to the problem.
   Determine the locked-in frequency with an accuracy of 1 kHz.

c) Measure the phase noise of the stabilized VCO and denote the values for every
   decade.
   Are there spurious signals? If so, where are they coming from?

5) Determining the lock time.

a) Measure the lock time of the PLL for a frequency jump from 10.8 GHz to 11.6 GHz
   and the other way around.
   Which measurement equipment can be used for this and what do you notice?

Settings of the RTO

Preset

Mode ⇒ Trigger Normal
Slope ⇒ Alternating
Trigger ⇒ Source ⇒ CH1
CH1 ⇒ as per expected values
Trigger level ⇒ as per Task 1, in the middle.

b) Adapt the measurement range and repeat the measurement for a frequency jump
   from 10.8 GHz to 12 GHz.
   What problem arises? How can this be solved?
6) Next set the VCO to a frequency of 10.48 GHz with the loop filter of 2\textsuperscript{nd} order.
   a) Is the PLL running in integer- or fractional-N-mode?
      Calculate the necessary division factor.
   b) Calculate the expected spurious frequencies. For this assume that the clock count for a cycle is $F=16\,777\,216$. Measure the noise peaks and compare them to the phase noise at integer-N-mode at 10.5 GHz.

   
   Preset
   \begin{align*}
   &\text{Trace} \Rightarrow \text{Copy Trace} \Rightarrow \text{Trace 1 after Trace 3} \\
   &\Rightarrow \text{Trace 2 after Trace 4}
   \end{align*}

   c) How can the spurious signals be suppressed?
   d) Repeat the measurements for the fractional-N-mode at 10.48 GHz for both loop filters of 3\textsuperscript{rd} order. Plot them both in a diagram. What’s the difference?

7) Use now the active loop filter.
   a) Repeat the measurements from problem part 5a) and discuss the results.
   b) How long is the lock time for a frequency jump from 10.8 GHz to 13.0 GHz?
   c) Increase the charge pump current to 5 mA.
      What do you expect to happen? Repeat problem part b).
   d) Measure the phase noise at 11 GHz with the now higher charge pump current and 13 GHz.