

# Full-Wave Design and Optimization of mm-Wave Diode-Based Circuits in Finline Technique

Werner Thiel and Wolfgang Menzel, *Senior Member, IEEE*

**Abstract**—This paper presents a full-wave design and optimization of a quasi-planar frequency doubler and a balanced subharmonic mixer in finline technique by applying the extended finite-difference time-domain (FDTD) method. The structures are based on the junction of a coplanar waveguide and a finline using two Schottky diodes mounted across this junction. The diodes are represented by their large-signal device circuit model. The specific problem of embedding the lumped elements in the FDTD mesh at millimeter-wave frequencies is discussed. A new method for the inclusion of the device into the grid is developed, avoiding nonphysical reactances. The frequency doubler is designed for optimal conversion loss at 0-dBm input power in a frequency band from 20 to 25 and 40 to 50 GHz, respectively. With the subharmonic mixer, matching structures at both the local-oscillator (LO) port and the radio-frequency (RF) port have been employed so that a conversion loss of 14.8 dB could be achieved with only 5-dBm LO power. The operation frequencies are 18 GHz for the LO and 56 GHz for the RF. The simulation results are validated by measurements.

**Index Terms**—FDTD methods, large-signal model, lumped elements, mm-wave frequency converters.

## I. INTRODUCTION

THE finite-difference time-domain (FDTD) method [1], [2] is successfully applied to the design and optimization of linear structures. Also, in recent years, nonlinear structures have been analyzed at microwave frequencies, and several methods for incorporating nonlinear devices into FDTD or modeling the device itself by finite-difference methods have been proposed [3], [5], [7].

With commercial computer-aided design (CAD) tools, the design of active circuits is limited and only successful for low frequencies and, in the special case, where the circuit approach is valid. The advantage of the CAD tools is that they possess an extensive library for various microwave and semiconductor devices. Computation time is short because the elements are cascaded with their scattering matrices one to another. Typically, however, no higher order mode coupling and no parasitic coupling between adjacent circuit parts are included. The limitations of standard CAD procedures are even more severe if the semiconductor device is placed directly in a major discontinuity and if it has, in addition, the same size as the junction. Also, as is shown later, the geometry and location of the device plays an important role for the parasitic effects and cannot be considered in a circuit approach. As a consequence,

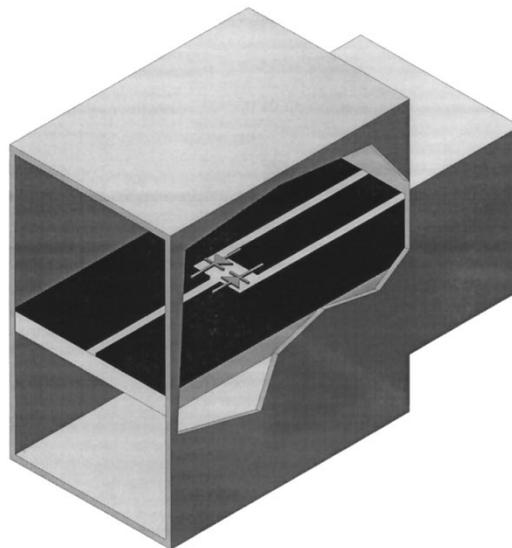


Fig. 1. Basic structure for frequency multiplication and frequency conversion.

a reliable analysis and optimization of the complete structure with such CAD tools becomes impossible. Without sufficient information, a circuit design in such problems is accomplished mostly in trial and error.

In this case, the extended FDTD method using equivalent-current source techniques is applied to model the complex circuitry, including quasi-planar structures as well as the diodes. The two diodes are described with their equivalent circuit and are embedded in the FDTD mesh in such a way that nonphysical parasitic effects are minimized. The influence of these effects in the millimeter-wave (mm-wave) range will be discussed in Section V.

## II. DESCRIPTION OF THE CIRCUIT

For broad-band operation, e.g., measurement systems, a balanced/unbalanced diode configuration has proven to be a useful concept for frequency multiplication of even order and for frequency conversion [8], [11]. Such a structure can easily be implemented in the junction of a coplanar waveguide and a finline, as shown in Figs. 1 and 2. The coplanar waveguide is placed in a waveguide channel of reduced cross section to reject the slot mode excited at the diodes. In the area of the junction of the coplanar line and the finline, a shielding with standard waveguide dimensions is used. In [6], such a junction was analyzed with the extended FDTD method. In this paper,

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The authors are with the Microwave Techniques Department, University of Ulm, 89069 Ulm, Germany.

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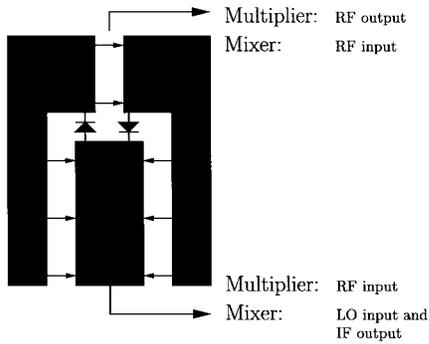


Fig. 2.  $E$ -field orientation and port definition for both applications.

an optimization of the complete circuit for a multiplier and harmonic mixer operation is presented.

### III. SIMULATION OF THE NONLINEAR STRUCTURES

Analyzing linear structures, a Gaussian pulse can be used for the incident signal and, with one simulation, the scattering parameters for the whole frequency band can be calculated. With nonlinear devices, a pulse excitation results in a rather complex harmonic spectrum not relevant for multiplier and mixer local-oscillator (LO) operation, thus a harmonic excitation has to be chosen. Consequently, for each frequency point and for each power level, an extra simulation is necessary. To calculate the quasi-linear conversion loss of a mixer, however, a modulated Gaussian pulse with a sufficiently small bandwidth can be used as an RF signal as soon as a steady state has been achieved for the harmonic LO excitation. The bandwidth of the pulse has to be chosen in such a way that a single-sideband operation of the mixer is guaranteed. With the mixer simulation, two sources (LO and RF signal) have to be included in the structure. Since the LO signal is not limited in time, a transparent source is required. For short feeding lines, as in this contribution, the natural field distribution is used for the excitation with the transparent source. As the LO signal has an amplitude 20 dB higher than the RF signal, for an extraction of the scattering parameters, two simulations of the mixer are necessary. In one simulation, only the LO signal is used. Thus, the RF signal can be calculated subtracting the signals of the two simulations, while the LO signal and its harmonics are cancelled.

In the mixer performance, sometimes sharp resonances can appear in the RF and IF signal, thus, for a reasonably accurate Fourier transformation, a large simulation time is necessary. An alternative is to use the system identification (SI) method described in [4]. In this way, the simulation effort can be reduced dramatically.

### IV. DEVICE CIRCUIT MODEL

As active devices, HP HSCH5330 silicon low-barrier Schottky diodes are chosen. The diodes were characterized up to 40 GHz at different bias states in two coplanar test circuits (Fig. 3) using an on-wafer prober and a vector network analyzer. In Fig. 3, the reference planes for a thru-reflection line (TRL) calibration are marked. The center conductor of the coplanar line has approximately the same width as the diode

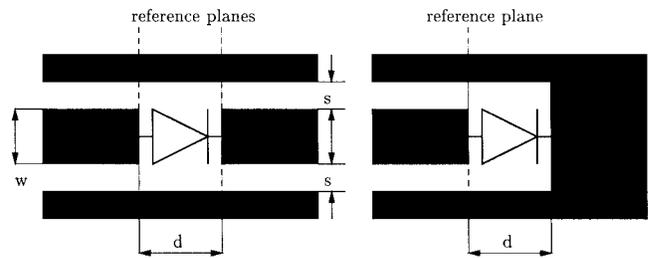


Fig. 3. Coplanar test structures:  $w = 200 \mu\text{m}$ ,  $s = 100 \mu\text{m}$ , and  $d = 300 \mu\text{m}$ .

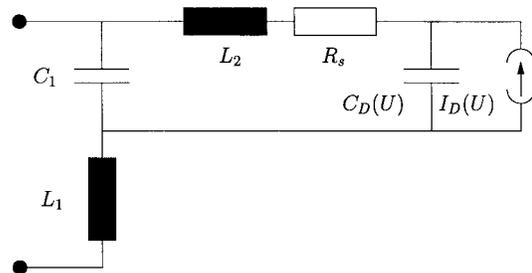


Fig. 4. Equivalent circuit of the diode. Element values:  $L_1 = 0.1 \text{ nH}$ ,  $L_2 = 0.04 \text{ nH}$ ,  $C_1 = 30 \text{ fF}$ ,  $C_{j0} = 60 \text{ fF}$ ,  $R_s = 10 \Omega$ , and  $I_0 = 10 \text{ nA}$ .

leads so that a discontinuity between the coplanar line and diode can be avoided. Using a commercial circuit simulator, the resulting scattering parameters were then fitted to a large-signal equivalent circuit, according to Fig. 4. The element values are listed in Fig. 4. The circuit includes two nonlinear elements, the Schottky junction capacitance  $C_D(U)$ , and the current source  $I_D(U)$ . Governed by the Schottky junction model, the Schottky junction capacitance is expressed as

$$C_D(U) = \frac{C_{j0}}{\sqrt{1 - \frac{U}{\Phi_0}}}$$

where  $C_{j0}$  is the capacitance at 0 V, and  $\Phi_0$  is the built-in potential. The current is described by the following equation:

$$I_D(U) = I_0 \left( e^{(qU/nkT)} - 1 \right)$$

where  $I_0$  is the saturation current and  $n$  the ideality factor. Investigations have shown that the nonlinear capacitance has a nonnegligible influence on the conversion loss and decreases it by up to 1 dB.

### V. LUMPED ELEMENTS IN THE MM-WAVE RANGE

In the literature, several approaches for an inclusion of lumped elements in the FDTD mesh can be found. In [3], the elements are regarded as dimensionless devices and are placed at the edge of a FDTD cell. In [5], the lumped element is a one-dimensional device between both conductors so that the device is distributed over several edges of the FDTD cells cascaded one by another. Dealing with low frequencies, (up to 20 GHz), such a way of inclusion does not have a remarkable influence on the electric behavior of the nonlinear microwave structure. In the mm-wave range, however, e.g., the  $V$ -band or even the  $W$ -band, nonphysical parasitic effects due to such

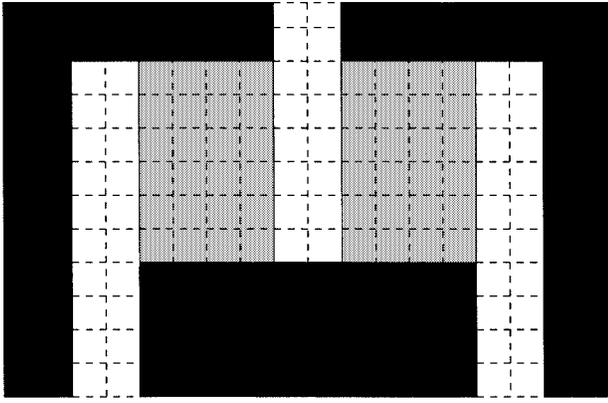


Fig. 5. Coplanar line–finline junction with the diodes in real size (dashed lines show the FDTD grid).

an incorporation of lumped elements will occur, resulting in erroneous computation results. In this section, the parasitic effects are characterized and validated by measurements. Following this, a solution will be shown how to embed the devices without the generation of nonphysical reactances.

The main problem at higher frequencies is that the device becomes as big as the passive discontinuity, thus, the size plays an important role. The device, as shown in Fig. 5, covers more than one FDTD cell and also most of the area of the junction. This has to be incorporated in the mesh structure. Four possible ways of including a diode into the FDTD mesh are indicated in Fig. 6, together with the corresponding equivalent circuits. Fig. 6(a), distributing the device linearly over several edges of cells, results in a nonphysical increased inductance twice as big as in reality, as the diode is included as a nonphysically very thin element only. In Fig. 6(b) and (c), metal pads are used to better model the physical size of the diodes. Typically, however, the equivalent circuit of the diode already includes the capacitance between the two diode leads; thus, this approach leads to an overestimation of capacitance. The best solution, therefore, is a distribution of the diode over the complete device area, i.e., Fig. 6(d). In this case, however, an increased numerical effort would be necessary for evaluating the nonlinear circuits for every FDTD cell. As a compromise, therefore, constant potentials are assumed over the contact areas of the diode—equivalent to a bigger mesh size in the diode area, and the equivalent circuit is now placed between these areas. The nonlinearity can be handled equally in all cells, or it equivalently can be placed again between the contact areas as a single lumped element (Fig. 7). If there is a complex lumped element or if the device is distributed over several cells in two dimension, it is advantageous to use the equivalent sources principle for the Ampere’s Law so that each cell can be described by

$$C_{\text{cell}}^{(i,j)} \frac{\partial U_{\text{cell}}^{(i,j)}}{\partial t} + I^j = I_{\text{total}}^{(i,j)}$$

with

$$\sum_{j=1}^m I^j = I_{\text{device}}$$

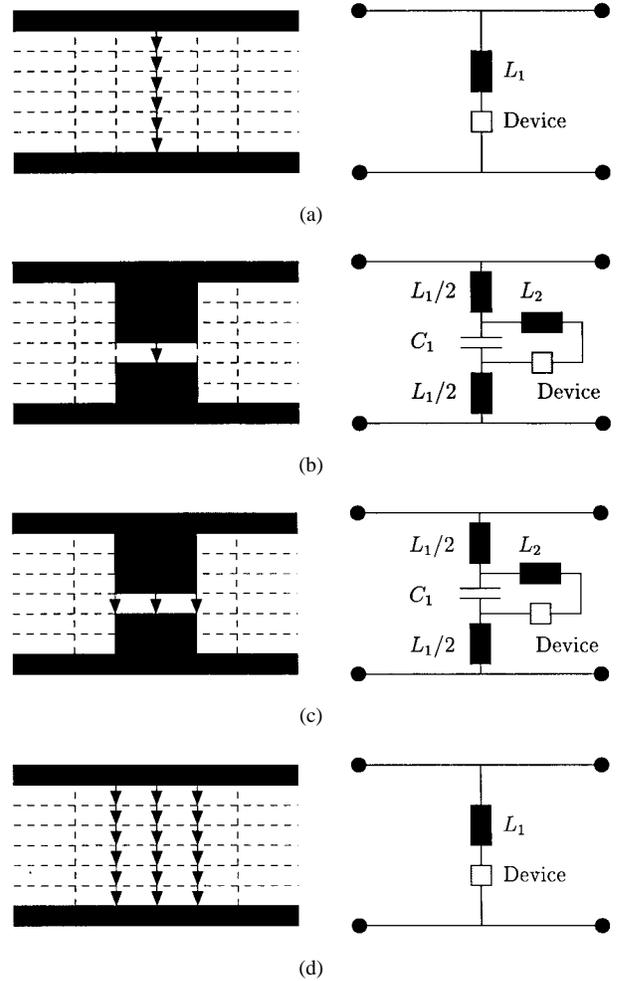


Fig. 6. Possibilities of incorporation of lumped elements; test structure: 220-Ω slotline with 300-μm slot width and V-band shielding (dashed line represents the grid 50 μm × 100 μm used for FDTD simulation). (a)  $L_1 = 0.204$  nH. (b)  $L_1 = 0.110$  nH,  $L_2 = 0.034$  nH,  $C_1 = 8.45$  pF. (c)  $L_1 = 0.110$  nH,  $L_2 = 0.013$  nH,  $C_1 = 8.45$  pF. (d)  $L_1 = 0.123$  nH.

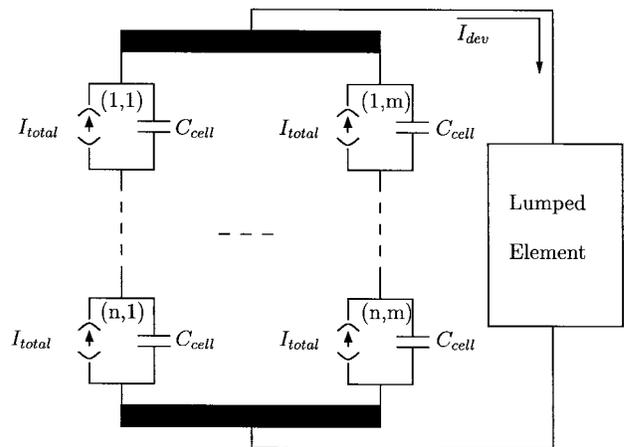


Fig. 7. The equivalent circuit governing the lumped element.

and

$$\sum_{i=1}^n U_{\text{cell}}^{(i,j)} = U_{\text{device}}$$

The circuit shown in Fig. 7 includes all FDTD cells and the lumped element. This approach is valid for the mm-wave range

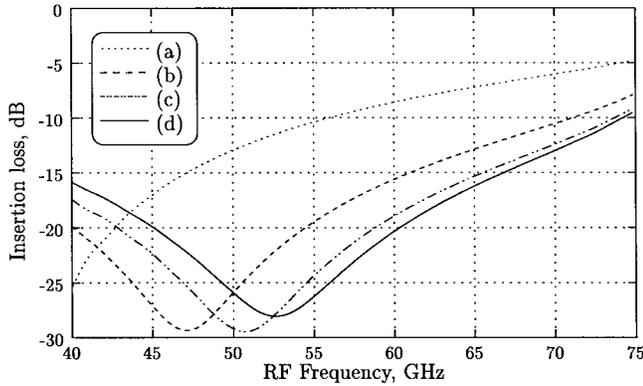


Fig. 8. Simulation of the test structure with four approaches for lumped-element inclusion (see Fig. 6).

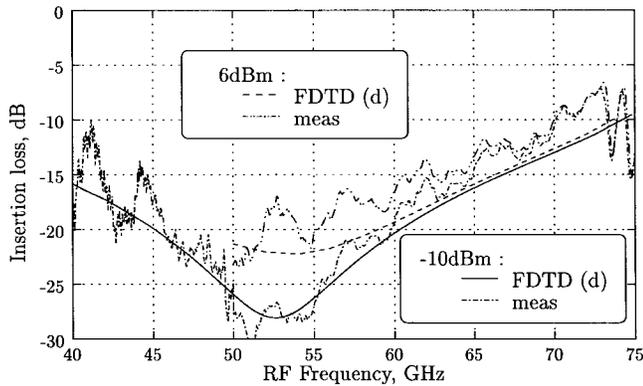


Fig. 9. Comparison of the simulated insertion loss Fig. 6(d) with measurements at  $-10$ - and  $6$ -dBm input power.

as long as the wavelength is much bigger than the width of the element. Otherwise, the device itself has to be simulated by full-wave methods itself.

Solving the circuit in Fig. 7, the following system of equations results:

$$\frac{\partial X}{\partial t} = A(X) + B$$

where  $X$  is the state vector including all electric-field components of the device area.  $A$  is derived from the circuit elements, and  $B$  represents terms of the sources  $I_{\text{total}}$ . Using centered differences to achieve a truncation error of second order, the system results in

$$\frac{X_{n+1} - X_n}{\Delta t} = A\left(\frac{X_{n+1} + X_n}{2}\right) + B + O(\Delta t^2).$$

The nonlinear system can be solved employing the Newton-Rhaphson method.

A test structure was fabricated to measure the diode properties and to validate this specific way of modeling of lumped elements. The diode is mounted across a finline slot in a  $V$ -band waveguide. In Figs. 8 and 9, measurements of small-signal scattering parameters at  $0$ -V bias are compared to the simulation results of the four approaches according to Fig. 6. At  $V$ -band the structure has a transmission minimum as the parasitic effects of the diode are in resonance. The diverse nonphysical reactances of the four ways for an inclusion of

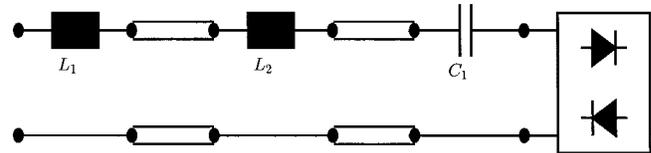


Fig. 10. Matching circuit for the frequency doubler:  $L_1 = 0.33$  nH,  $L_2 = 0.83$  nH,  $C_1 = 1.8$  pF.

the diode lead to different resonance frequencies (Fig. 8). The insertion loss was measured at  $-10$ - and  $6$ -dBm input power. Between  $40$  and  $50$  GHz, a power level of  $6$  dBm was not available. If the model according to Fig. 6(d) is used, good agreement between the measurements and simulation is achieved (Fig. 9). Thus, the approach presented above is sufficient for the mm-wave application.

## VI. OPTIMIZATION OF A FREQUENCY DOUBLER

For a better return loss, i.e., an improved conversion loss of the multiplier, a matching network was designed. The operation frequencies should be  $20$ – $25$  and  $40$ – $50$  GHz, respectively. The input power of the frequency doubler is chosen to  $0$  dBm.

With nonlinear structures in the large-signal operation, it has to be taken into account that the diode impedance depends strongly on the input power. The power directly at the diodes, however, is correlated to the input reflection coefficient. Therefore, the diode impedance will vary if a matching circuit is employed, and the input power is unchanged. For the extraction of the scattering parameters of the junction, the power level has to be adjusted so that, at the diodes, the same power level as in the matched case is guaranteed. In the case of complex matching structures, where the condition for constant power at the diodes cannot be fulfilled, several iterations for the design of a matching structure may become necessary. In this contribution, however, no iterations were necessary.

The characteristic impedances of the coplanar waveguide and of the finline are  $50$  and  $110 \Omega$ , respectively. The first simulations showed that the smaller the characteristic impedance of the finline, the better the conversion loss. The value of  $110 \Omega$  is the lower limit due to the available technology. For impedance matching, a Chebyshev-type filter is applied. The junction with the two diodes is the first element of the three-section filter. This leads to a bandwidth of  $3.6$  GHz with an equal ripple response of the return loss of  $-9.4$  dB. In a CAD tool,<sup>1</sup> the filter circuit according to Fig. 10 is used for a preliminary design of the inductances and capacitance of the inverters, which then are used as starting values for the next optimization step. The inverters are realized in coplanar technique and are analyzed and optimized with FDTD using a gradient approach. The geometries of the coplanar inverters were varied in discrete steps according to the relatively fine discretization until the desired transmission is achieved. The scattering matrices of the inverters based on the full-wave simulation are included in the CAD tool together with the nonlinear part. In that way, the resonator lengths can

<sup>1</sup>MDS (Microwave and RF Design System), version 7.1, Hewlett-Packard Company, Santa Rosa, CA.

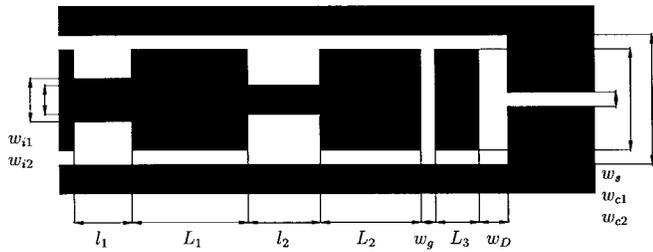


Fig. 11. Layout of the matching network for the frequency doubler. Dimensions:  $w_{c1} = 1.2$  mm,  $w_{c2} = 1.45$  mm (coplanar waveguide),  $w_s = 0.05$  mm (slotline),  $w_D = 0.35$  mm,  $L_3 = 1.732$  mm (first section),  $w_g = 0.08$  mm (capacitive inverter),  $L_2 = 4.803$  mm (resonator),  $l_2 = 1.2$  mm,  $w_{i2} = 0.1$  mm (inductive inverter),  $L_1 = 5.961$  mm (resonator),  $l_1 = 0.4$  mm,  $w_{i1} = 0.2$  mm (inductive inverter).

quickly be optimized. If the optimized amplitude response of the filter deviates from the theory, inverters with a slightly different transmission can be inserted. The optimization of the resonators and modification of the inverters has to be repeated until the desired amplitude response is achieved. The doubler, including the matching network as a whole, is then analyzed by FDTD method, and the return loss is compared to the expected one. In Fig. 11, the matching network and its geometry are plotted. Comparing the measurement and simulation result (Fig. 12), the conversion and return losses show good agreement. The bandwidth is larger than predicted. The return loss is below  $-10$  dB in a 5.5-GHz range. Compared to the frequency doubler without matching network, the conversion loss could be improved by about 3 dB (Fig. 13), and the return loss by about 7 dB (Fig. 12). The optimized doubler is relatively nonsensitive with respect to the input power. Decreasing the input power by 3 dB, the return loss rises to  $-7$  dB (Fig. 14). The simulation has shown that the bandwidth becomes smaller with increasing power. At 6-dBm input power, the bandwidth is reduced by about 1 GHz. The frequency shift in the measurement is caused, on one side, by some fabrication tolerances of both the passive structure and diodes. A further reason is the low discretization of the structure for the theoretical analysis. Otherwise, the simulation time is too long for a reasonable optimization. For the FDTD simulation, the doubler was divided into 350 000 cells. For an extraction of the scattering parameters from the harmonic time signal, 16 000 time steps were required. On a Pentium II, 100-min central processing unit (CPU) time was needed for one frequency point.

## VII. DESIGN OF A V-BAND SUBHARMONIC MIXER

In the V-band, a subharmonic mixer with both a matched LO and RF port was designed. The incorporation of the diodes in this frequency band is much more delicate than with the doubler in the B-band. An accurate large-signal device circuit and the elimination of nonphysical reactances is important for a successful full-wave analysis. In this application, a good conversion loss had to be obtained even with a low LO power level (available LO power: 5 dBm in this case). Therefore, an LO and RF matching network is mandatory. Without a matched LO port, the conversion loss achieves its minimum at 9-dBm LO power. At 5-dBm input power, the LO return loss

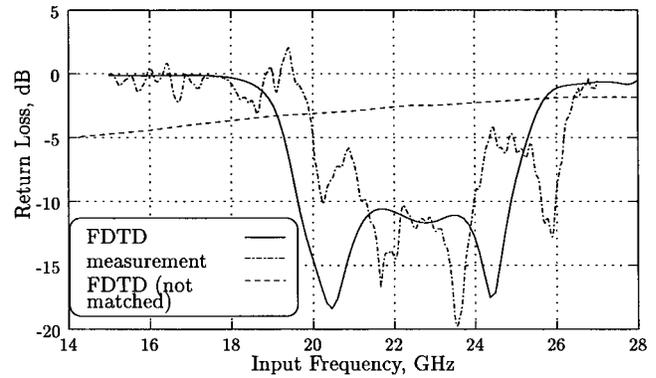


Fig. 12. Input return loss of the frequency doubler at 0-dBm input power.

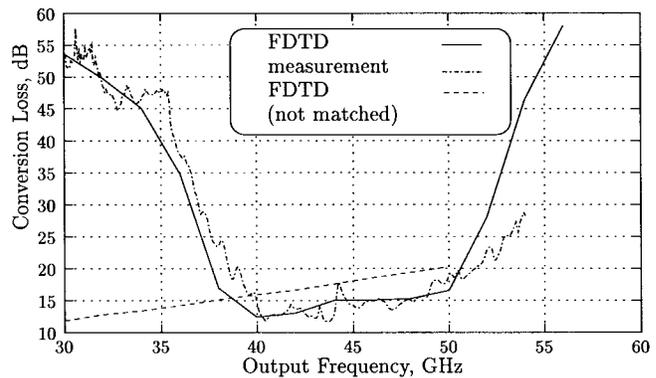


Fig. 13. Conversion loss of the frequency doubler at 0-dBm input power.

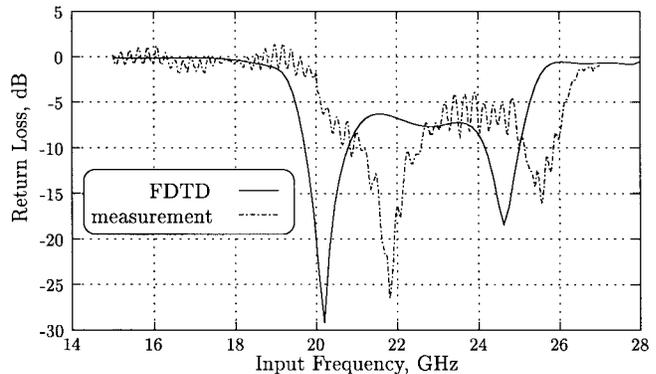


Fig. 14. Input return loss of the frequency doubler at  $-3$ -dBm input power.

then is  $-4.8$  dB. The geometry of the LO matching structure is shown in Fig. 15. The quarter-wave transformer consists of a transmission line with ground metallization for a low characteristic impedance. The resulting return loss of the LO port is shown in Fig. 16. A return loss of  $-15$  dB could be achieved over a 3-GHz bandwidth.

Before describing the RF matching network, a few properties of the mixer have to be discussed. Since the diodes are mounted in series with regard to the finline, the RF signal generates a slot mode on the LO coplanar line of the mixer. Therefore, the LO matching network is not only a quarter-wave transformer for the LO signal, but also a linear complex load for the slot mode of the RF signal. In this way, the RF return loss is affected by the LO matching network. Furthermore, the

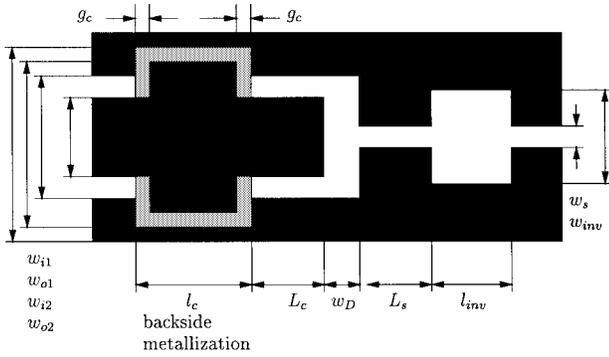


Fig. 15. Layout of the central part of the harmonic mixer matched at both ports. Dimensions:  $w_{i1} = 0.7$ ,  $g_{01} = 0.5$  (coplanar waveguide);  $w_{i2} = 1.3$  mm  $w_{o2} = 1.5$  mm (coplanar waveguide inverter);  $l_c = 1.8$  mm,  $L_c = 0.5$  mm,  $g_c = 0.2$  mm (coplanar inverter).  $w_s = 0.1$  mm (slotline).  $w_D = 0.3$  mm,  $L_s = 0.9$  mm,  $w_{inv} = 0.7$  mm,  $L_{inv} = 1$  mm (slot inverter).

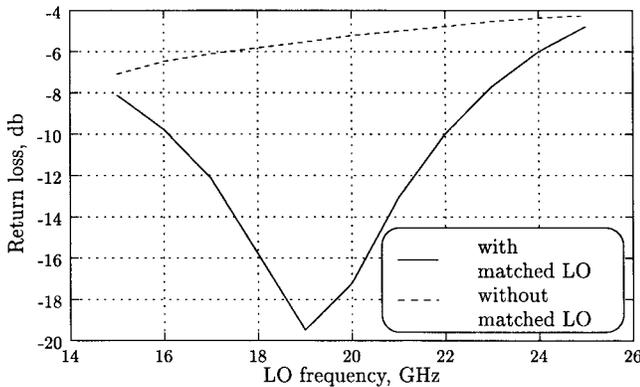


Fig. 16. Return loss of the matched LO input at 5-dBm input power and of the unmatched LO at 7-dBm input power.

slot-mode propagating on the coplanar line has to be rejected so that the cross section of the shielding is reduced behind the LO matching circuit. In this part of the coplanar waveguide, resonances may occur by the slot mode. They are caused by the LO circuit and the position of the reduced shielding. The effect of such resonances is that the IF signal nearly disappears. As a consequence, by proper design of the position of the waveguide section with the reduced dimensions, the resonance has to be shifted out of the operation band. The resonance in RF return loss is visible in the FDTD simulation, but not in the measurements due to losses. With this mixer, the resonance is at 58.5 GHz. (A return loss greater than 0 dBm at about 58 GHz is an artifact of the SI method only.) Measurement and simulation, however, show that the conversion loss increases accordingly at 4.5-GHz IF frequency. Without any matching networks for both ports, at 5-dBm LO power, a conversion loss of 19 dB can be obtained. Using an RF matching structure, as shown in Fig. 15, the constant return loss of  $-2.8$  dB could be improved to  $-10$  dB in a bandwidth of 3 GHz (Fig. 17). Fig. 18 shows the conversion loss of the optimized mixer. The conversion loss could be reduced to 14.8 dB at 2-GHz IF frequency.

Investigations show that the return loss of the mixer is very sensitive to deviations in parasitic effects like the feeding

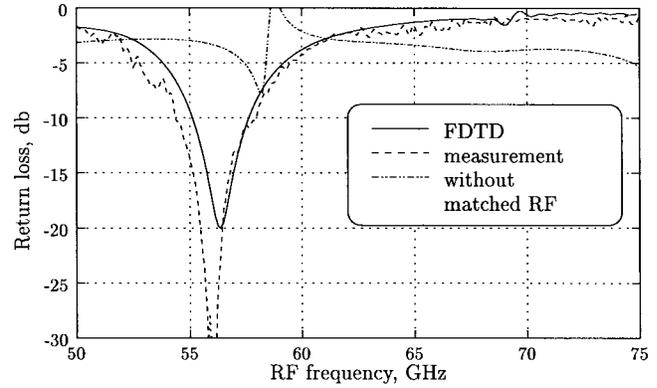


Fig. 17. RF return loss of the harmonic mixer at  $-5$ -dBm input power and 5-dBm LO power.  $f_{LO} = 18$  GHz.

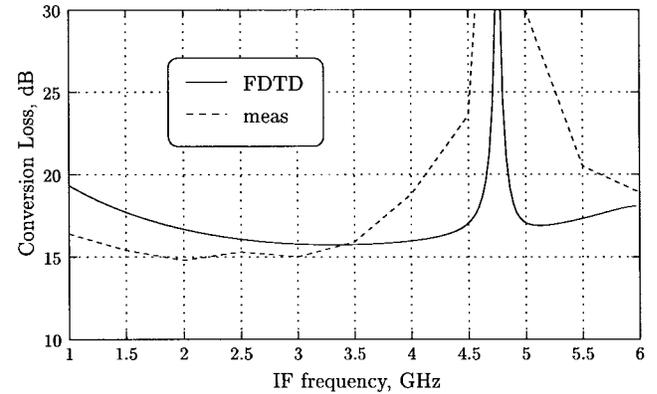


Fig. 18. Conversion loss of the harmonic mixer at  $-5$ -dBm input power and 5-dBm LO power.  $f_{LO} = 18$  GHz.  $f_{RF} = 55$ -60 GHz.

inductance. For an example, if the width of the diodes is reduces by  $50 \mu\text{m}$  in the FDTD simulation, the optimal operation frequency is shifted by 4-52 GHz. Also, if the gap between slotline and coplanar waveguide is reduced to  $200 \mu\text{m}$ , the lower inductance causes a frequency shift of 3 GHz. This shows that the modeling of the diode and a good mechanical accuracy are critical points in this frequency range.

VIII. CONCLUSION

In this paper, an optimization of mm-wave diode-based circuits is presented. For higher frequencies, e.g., in the V- or W-bands, a concept for the incorporation of lumped elements in the FDTD mesh without generating nonphysical reactances has been presented. As an example, a frequency doubler was designed for optimal conversion loss at 0-dBm input power. Furthermore, a subharmonic mixer with 18-GHz LO frequency and 56-GHz RF frequency was optimized with respect to a low conversion loss for low LO power. The FDTD method has proven to be a useful tool for the design of nonlinear components even in the mm-wave range.

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**Werner Thiel** was born in Altötting, Germany, in 1970. He received the Dipl.Ing. degree from the University of Ulm, Ulm, Germany, in 1995, and is currently working toward the Ph.D. degree in microwave techniques.

Since 1995, he has been with the Microwave Techniques Department, University of Ulm. His research activities and interests include the finite-difference techniques in general, development of FDTD software, and the design and optimization of nonlinear components in the millimeter wave

applying the FDTD method.

**Wolfgang Menzel** (M'89–SM'90), for photograph and biography, see this issue, p. 2241.