PROPOSAL OF A NEW LANDING AREA FOR SAW RF FILTERS IN WIRELESS APPLICATIONS ENSURING PRECISELY PREDICTABLE FILTER CHARACTERISTICS

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Abstract — **Due to the high complexity and the high performance of packaged SAW RF filters, it is extremely difficult to guarantee comparable performance of them on different printed circuit boards (PCBs) and in the final application environment.**

This paper presents a new approach of designing physical different PCBs such that SAW RF components on them exhibit identical performance. The new approach is based on the concept of using optimized test environments, i.e., test environments with minimal reflections, minimal cross-talk, and minimal losses, in order to obtain the pure filter characteristics. The applicability and advantages of the new approach are exemplified.

I. INTRODUCTION

Surface acoustic wave (SAW) radio frequency (RF) filters are key components in the RF sections of mobile communication equipment. Over the past years, the size of the packages has decreased from a typical form factor of 5.8 mm x 5.8 mm to 1.4 mm x 2.0 mm, and center frequencies have shifted from 1 GHz to above 2 GHz. At the same time further functionality has been added to the pure filtering function. Examples of such additional functions are impedance transformation or balun functionality to handle balanced signals. Besides, the permanent pressure for quality enhancements in the field of wireless communication has driven manifold step-by-step improvements of the filter performance regarding matching, close-in and far-off selectivity, and pass band attenuation.

Driven by these trends, the accurate determination of the electrical characteristics of SAW RF filters has become a critical prerequisite for their efficient design. Up to now it is still a problem that the measurement environment, in particular, the PCB on which the component is soldered for operation, can significantly influence the measured electrical characteristics [1].

In [1] a new test PCB has been proposed. Its design has been optimized towards minimal reflections, minimal feed-through or cross-talk, and minimal losses. Thus, the measured data of a SAW filter on this PCB is only minimally influenced by the electrical characteristics of the PCB. This is a prerequisite for test PCBs, which are used to check the agreement of the performance of a SAW RF filter with its specifications.

In the application environment, the electrical properties of the filter differ at least slightly to the measured characteristics on the test PCB. The deviations result from physical differences in the layer stacks and the metallization patterns of the two PCBs.

In the paper a new design for the landing area on the application PCB will be given, which offers the same optimized electrical properties as the landing area on the previously described test PCB in spite of the different layer stacks. Thus, the performance of the filter in the application is precisely predictable by measurement results obtained on the test PCB.

Sec. II starts with an example comprising a couple of SAW filter setups that emphasizes the potential impact of PCBs on the electrical filter characteristics. Sec. III shows measures to avoid these effects leading to the proposal of a new landing area for the PCB in the application environment with results being given in Sec. IV. Sec. V summarizes and concludes the paper.

II. CHARACTERIZATION OF RELEVANT EFFECTS BY MEASUREMENT AND SIMULATION

Fig. 1 shows the measurements of a SAW RF filter mounted on different test setups. In addition, a simulation of one of these test setups is included, showing excellent agreement with the corresponding measurement of the setup. Therefore, all electrical properties of the simulated component have been taken into account sufficiently. Consequently, in Sec. III and IV simulation results will be used to prove the given approach. The simulation has been obtained using techniques according to [2], [3], [8]-[16].

The measurement setup comprises the following parts. At the connection interface for the measurement equipment the test setups consist of the subminiature type A (SMA) connectors, mounted on the test PCBs and realizing the coaxial line to microstrip line (MSL) transition. The MSLs lead to the landing area onto which the filter is soldered. The landing area comprises the planar metal structures and vias of the upper layers down to the first solid metal ground layer.

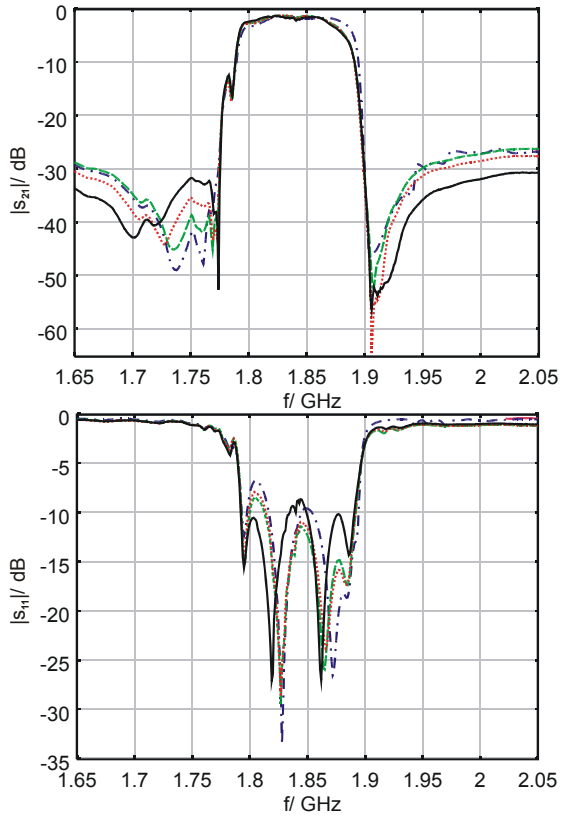

Fig. 1: Measured scattering parameters of identical filters on three different PCBs ((1) green-dashed, (2) red-dotted, (3) black-solid) and simulated values (blue-dash-dotted) of the same filter on the PCB used for measurement (1).

Naturally, parasitic effects inside the dielectric layers and in the signal and ground paths of the PCB, like parasitic coupling, depend on the different PCB designs. The effects influence the measurement result for the SAW RF filter in the test setups, as shown in Fig. 1. The plotted data for the three PCBs show several differences. For example, the close-in and far-off selectivity levels change significantly and, also the matching characteristic alters.

III. Design of an Optimized Quasi-Application PCB

In a first step, the effects of the SMA connectors, the transitions from SMA connectors to MSLs, the MSLs, and the landing areas for the devices under test (DUTs) were precisely investigated aiming at an optimal design of the test and application PCBs. The investigations have been done by simulation using commercial EM field simulators. The simulation has been experimentally verified with a suite of well-known, measured test configurations.

Table I
Dimensions and properties of 50 Ω microstrip line used for the test PCB (a) and the quasi-application PCB (b).

PCB design	(a)	(b)	unit
Substrate height h_1 of 1st (top) layer	200	60	µm
Substrate height h_2 of 2nd layer	-	135	µm
line width w	340	100	µm
metal thickness t	35	17	µm
height of solder resist s	0	0	µm
relative permittivity ε_r	4.5	4.5	
Line impedance Z	50	50	Ω

The electrical properties have been optimized in order to yield a test PCB causing minimal reflections, minimal feed-through or cross-talk, and minimal losses. We then transferred the results to a quasi-application PCB. Due to the modified layer stack the landing area had to be redesigned as described below. The specifications of the layer stacks are listed in Table I. It should be noted that the height of the top dielectric layer of 60 µm is very similar to that of the phone PCBs and, thus, the application environment.

The reduction of the layer height requires several changes in the layout of the landing area. Firstly, in order to achieve a characteristic impedance of the MSLs of 50 Ω, the line width has to be reduced from 340 µm to 100 µm.

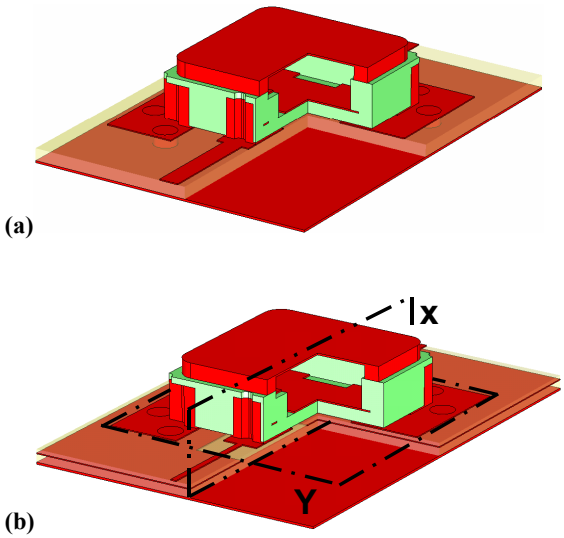

Fig. 2: Simulation models of the optimized test (a) and the new quasi-application (b) environment with mounted ceramic SAW filter package.

Secondly, a strong field discontinuity in the signal path is generated by the step in width from the microstrip line to the soldering pad. As a size reduction of the soldering pad is not possible due to the predetermined solder pad size of the SAW component and the positioning tolerances of the pick and place machines, an attempt has been made to reduce the effect of the discontinuity at the soldering pads by cutting out the areas in the upper inner ground layer below the soldering pads. Thus, the second inner metal layer is used as the actual ground plane below the soldering pad.

Landing area designs for an optimized test PCB and an optimized quasi-application PCB are given in Figs. 2a and 2b. As an example a well-known ceramic 3 mm x 3 mm package has been chosen.

A cross-section view of the field distribution of the electric field is given in Fig. 3, showing a uniform field distribution between the MSL and the package within the optimized landing area. In order to avoid field fringing and to guarantee optimized properties of the PCB, both size and position of the cut-out area have to be chosen carefully as indicated below.

The size of the cut-out area has to be realized in a way ensuring that the main part of the electromagnetic field below the soldering pad goes to the second ground layer. Thus, field components towards the edges of the cut-out in the upper ground layer have to be avoided. An undersized cut-out area will lead to almost unchanged field fringing as without cut-out.

Special focus has to be put on the front edge of the cut-out towards the microstrip. Its position must be chosen close to the soldering pad. Otherwise, an additional MSL with high characteristic impedance, altering the properties of the SAW component, will be unintentionally constructed by cutting away the original ground plane of the microstrip line. The result is a microstrip line of short length with very high characteristic impedance in the signal path, showing inductive behavior. A plot of the target field distribution in the cut-out area is given in Fig. 4a.

Another important point during optimization is the provision for an undisturbed current path. See Fig. 4b. Hereto, a sufficient number of vias has to be positioned in the ground structures on top of the PCB in the vicinity of the MSLs.

It should be noted that during the layout process, general design guidelines, as given in [1], have to be taken into account. To avoid field propagation by parallel plate modes between the inner ground layers of the PCB, a sufficient number of ground vias has to be implemented. A technique using vias for this purpose is given in [4], [5]. Under certain circumstances, this effect can lead to parasitic coupling, PCB resonances, or radiation on the outside of the PCB.

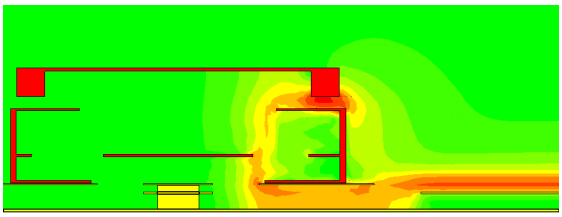

Fig. 3: Magnitude of the electric field in the central cross-section (x-plane, Fig. 2b) of the quasi-application PCB . The thickness of the top dielectric layer relevant for the MSL can be guessed from metal distance at the central via.

IV. Results

For validation purposes, the same filter as already used in Sec. II, has been simulated on both PCB structures shown in Fig. 2 again using techniques explained in [2]. In Fig. 5 simulation results of this filter on the previous test PCB and on the new quasi-application PCB are given. The plotted curves indicate excellent agreement of the electrical characteristics with respect to close-in and far-off selectivity and reflection attenuation. Differences resulting from parasitic effects in the PCBs, as explained in Sec. II (Fig. 1), do not occur in Fig. 5. Thus, the concept of a landing area design for application PCBs, having the same optimized electrical characteristics as on an optimized test PCB, has been proven.

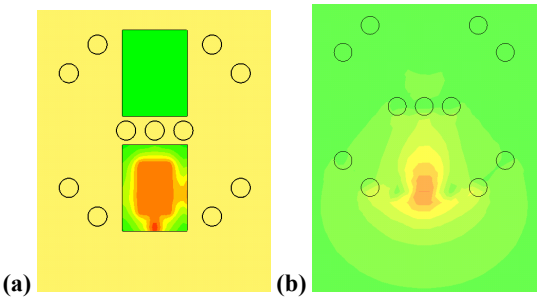

Fig. 4: Magnitude of the electric-field on the upper ground layer (a) and of the current density on the second ground layer (b) of the quasi-application PCB (y-plane, Fig. 2b).

V. Conclusion

The paper has proven the new concept of PCBs showing that optimized test PCBs for testing SAW RF components and optimized application PCBs for operating SAW RF components allow to yield the same performance of the components. It has been shown, that this is possible despite the fact that the two environments exhibit considerable

physical differences regarding their layer stacks, for instance. The most important prerequisites have been the electrical properties of the PCBs, i.e., that the test PCBs show minimal reflections, minimal cross-talk, and minimal losses. In order to prove the concept, a quasi-application PCB representing the final phone PCB has been designed and evaluated. A proposal for the landing area of an application PCB and, thus, for a phone PCB is given and discussed in detail.

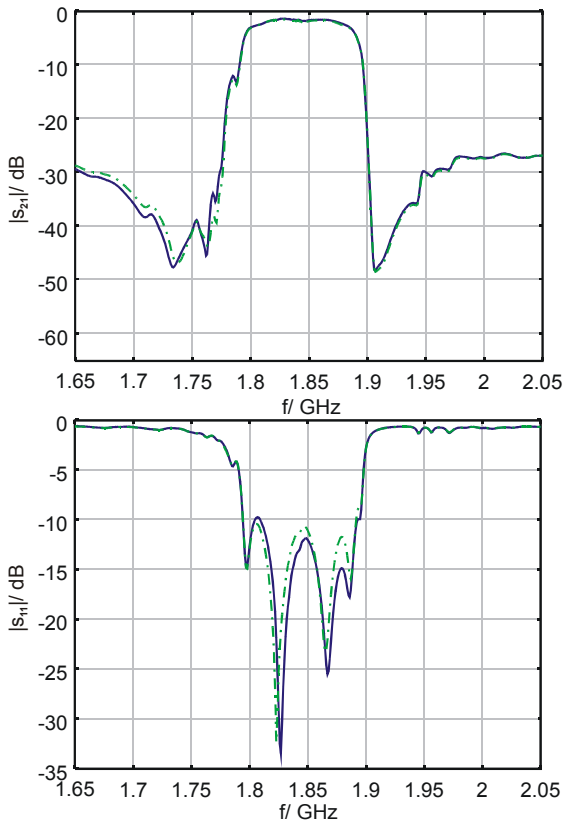

Fig. 5: Comparison of simulated scattering parameters of identical filters on optimized test PCB (green, dash-dotted) and new quasi-application PCB (blue, solid).

VI. REFERENCES

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