Integrated RF Front-End in 0.13 μm CMOS for Automotive and Industrial Applications beyond 20 GHz

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Student Paper

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Abstract

An integrated front-end, for automotive and industrial applications beyond 20 GHz, in 0.13 μm standard CMOS is presented. The front-end chip includes a low noise amplifier, a transformer-based Gilbert-mixer, an intermediate frequency amplifier and a buffer for the local oscillator input. The differential front-end at 22.5 GHz, measured on test-board, achieves a gain of 25.8 dB, a SSB noise figure of 6.8 dB, an input IP3 of -34.6 dBm and an input 1 dB compression point of -41.5 dBm while consuming 112.5 mW at a power supply voltage of 1.5 V.

Introduction

The majority of Radio Frequency (RF) integrated circuits are implemented in GaAs or silicon bipolar technologies due to their high unity-gain cut-off frequency (f_t), hence historically used for high-speed applications [1] [2]. However, one of the problems of implementing high frequency systems with such a material is the high cost associated with it. For RF circuits operating above 20 GHz, CMOS offers cost-effective and single-chip solutions with potential for radar and wireless communications systems [3]. An integrated CMOS chip which combines elementary RF building blocks, such as a low noise amplifier (LNA) and a down-conversion mixer, is called the front-end of an RF receiver. The input noise of the front-end must be sufficiently low in order to detect the weakest of input signals. Also, the gain of the receiver must be high enough to fulfill the requirements of wide input dynamic range. The purpose of this work is to develop a CMOS receiver front-end operating at frequencies above 20 GHz either for a vehicle radar application such as a car-to-car communication system or industrial sensor applications.

Front-End Architecture

Fig. 1 depicts the block diagram of the proposed CMOS front-end which consists of an LNA, local oscillator (LO) buffer, a transformer-based Gilbert-mixer and an intermediate frequency (IF) amplifier. The concept of the dual conversion, as shown in the block diagram, exhibits a large frequency separation between the RF and LO frequencies [4] and avoids the generation of I/Q signals at the first LO frequency. This receiver architecture also mitigates additional IF filters by using high IF. Additionally, implementation of only one voltage controlled oscillator (VCO) is one of the key features for high level integration. Furthermore, simple L-C tank at the mixer output are inserted for IF filtering.

The fully differential receive chain provides an IF-interface at a more easy to handle frequency range of 4.8 GHz. The LNA and mixer together determine the performance of the front-end. Although a large LNA gain is desirable, too large gain may overload the mixer and compromise dynamic range. On the other hand, the gain must be large enough to overcome the fundamentally higher mixer noise. It is also preferable to connect the LNA to the mixer input in some simple way, without the inclusion of high power consuming RF buffer circuit.

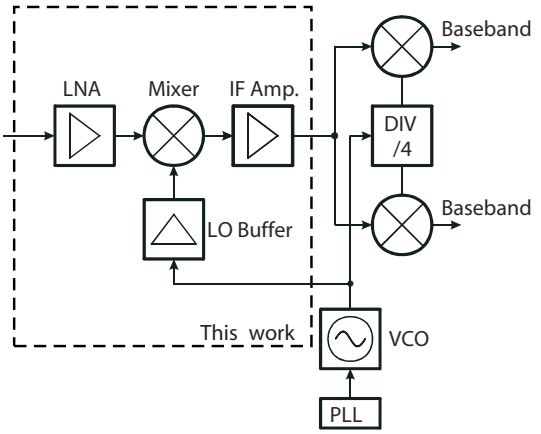

Fig. 1. Block diagram of the presented front-end.

Circuit Implementation

A. LNA Design

A fully differential common-source type LNA with on-chip inductive degeneration is chosen. LNA-design is one of the main challenges in the front-end design, since this circuit determines the total noise figure of a receiver. The LNA core in Fig. 2 consists of a cascoded, inductively degenerated common source input stage that converts the available power into a current. This topology allows reasonable input matching with a low noise figure and low power consumption. The inductive degeneration, employed at the common source node of the LNA, achieves a real valued input impedance. The cascode device lowers the output conductance, making the gain dependent only on the load network. Also, the cascode device reduces the Miller effect on the capacitance C_{gd} by ensuring a low impedance at the drain of the amplifying device. Therefore, the cascode improves the reverse isolation of the LNA, thus reducing the LO leakage.

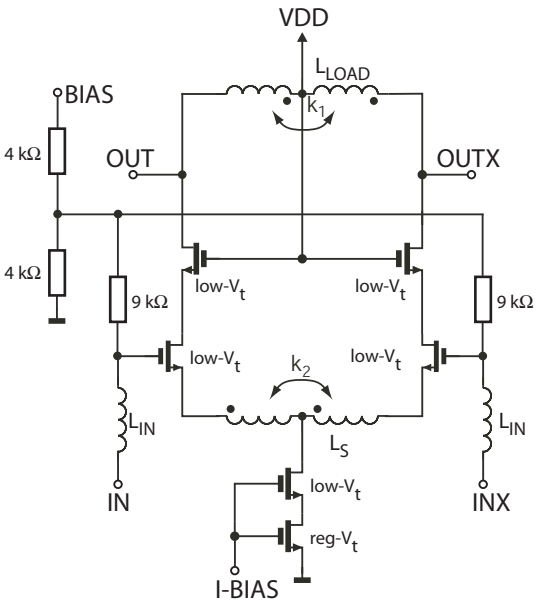

Fig. 2. Simplified schematic diagram of the LNA.

The LNA-output is loaded by an integrated LC-tank to improve the gain. In order to achieve a high quality factor in the LC-tank, it is necessary to minimize the total capacitance and maximize the inductance. Therefore the total capacitance seen by the inductor in the circuit is realized by parasitic capacitance. Furthermore, this tank provides a bandpass filter characteristic at 24 GHz. The integrated series inductors at the input of the LNA improves the input matching as well as the high-frequency gain in a robust way as compared to external matching or bond wire matching. All inductors are precisely integrated without significant area penalty at an operational frequency of 24 GHz (see chip photograph Fig. 5).

B. Mixer Design

The amplified signal at the LNA output is down-converted to a intermediate frequency of 4.8 GHz for further amplification, filtering and detection. The down-conversion mixer, schematic diagram presented in Fig. 3, is an integral part of the RF front-end. The classical double-balanced Gilbert type mixer [5] is considered as the best solution to combine acceptable gain, noise figure and linearity. To obviate the problems caused by the low supply voltage of 1.5 V for the 0.13 μm CMOS process, a fully differential integrated transformer [6] was inserted between the input transconductance stage and the switching pairs. Power supply is connected to the center tap of primary winding of the transformer while the center tap of secondary winding is grounded. This topology effectively doubles the voltage headroom available for the circuit design and additionally enables the insertion of cascode transistors to control the linearity and current in the mixer switching stage.

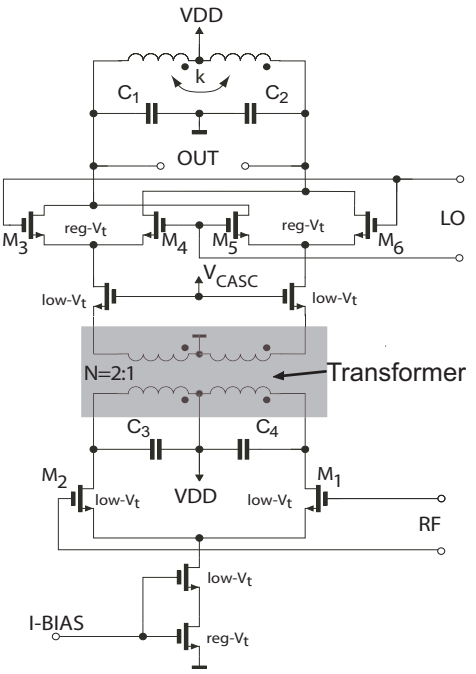

Fig. 3. Simplified schematic diagram of the Mixer.

To achieve the highest coupling between the two stages, the transformer resonates at the desired center frequency of 24 GHz by the inclusion of two NMOS-capacitances to the primary winding. Further, the mixer is loaded by an integrated LC-tank at 4.8 GHz to enhance the gain and to provide second order bandpass filtering. In order to achieve the maximal inductance per chip area, the inductor is realized as a cross-coupled fully differential inductor. The total capacitance seen by the inductor in the circuit is realized with the inherent capacitance of the inductor (inner winding and to substrate) and the capacitance of the connected transistors (drain, gate). Also, the parasitics of the interconnections must be considered, especially between two stages. The integrated inductor of

the tank circuit, with differential topology, has an inductance of 5 nH. Fig. 4 shows the lumped double π-model of the used inductor.

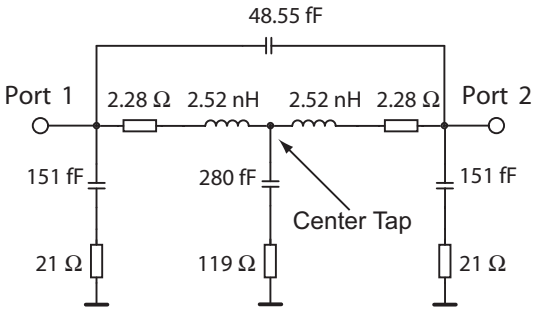

Fig. 4. Schematic of the 5 nH inductor.

Experimental Results

The front-end is realized in a standard 0.13 μm six-metal-copper CMOS process of INFINEON [7]. Fig. 5 shows the chip photograph with a die area of 0.80 mm^2. The front-end is characterized using chip-on-board mounting. The measurement results which includes the parasitics of the bondwires and the losses of Rogers RO 4003 substrate test-board (substrate thickness = 0.51 mm, dielectric constant $\varepsilon_r = 3.38$), are summarized in Table I.

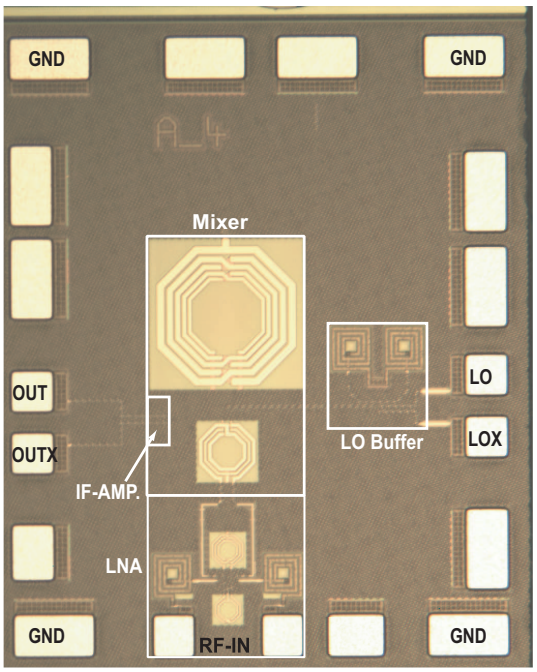

Fig. 5. Receiver front-end chip photograph. (Die size 800 μm × 1000 μm)

All measurements were performed at 1.5 V supply voltage with a total power consumption of 112.5 mW. Fig. 6 presents the measured gain as a function of RF input frequency with LO frequency 4.8 GHz apart and an external LO power of 3 dBm. A shift of resonance frequency at the primary side of the transformer, deployed

TABLE I
Receiver front-end performance summary at 22.5 GHz RF frequency, 17.7 GHz LO frequency and 3 dBm LO input power.

Power supply	1.5 V
Total power consumption	112.5 mW
LNA power consumption	19.5 mW
Mixer power consumption	45 mW
LO-Driver power consumption	19.5 mW
IF-Amplifier power consumption	28.5 mW
IF frequency	4.8 GHz
Power Gain	25.7 dB
Noise Figure SSB	6.8 dB
Input compression point	-41.5 dBm
Input IP3	-34.6 dBm
Die Area	0.80 mm^2
Technology	0.13 μm standard CMOS

in mixer (refer Sect. Mixer Design), is a plausible explanation i.e the transformer is intended to resonate at 24 GHz but due to additional parasitic capacitances of the layout, it resonates at 22.5 GHz. The measured noise figure is also shown in Fig. 6. The receiver front-end achieves a SSB noise figure of about 6.8 dB.

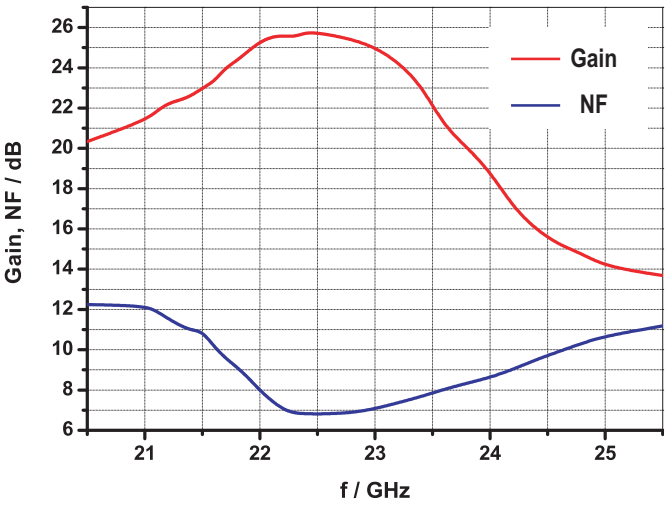

Fig. 6. Measured gain and noise figure over frequency at a fixed IF frequency of 4.8 GHz.

The 1 dB input compression point was measured for a LO input frequency of 17.7 GHz and a RF input frequency of 22.5 GHz. The single-tone compression measurement result is presented in Fig. 7. The 1 dB input compression point is -41.5 dBm. The two-tone intermodulation measurement results are presented in Fig. 8. The distance between the tones is 1 MHz. The front-end features a measured input IP3 point of -34.6 dBm.

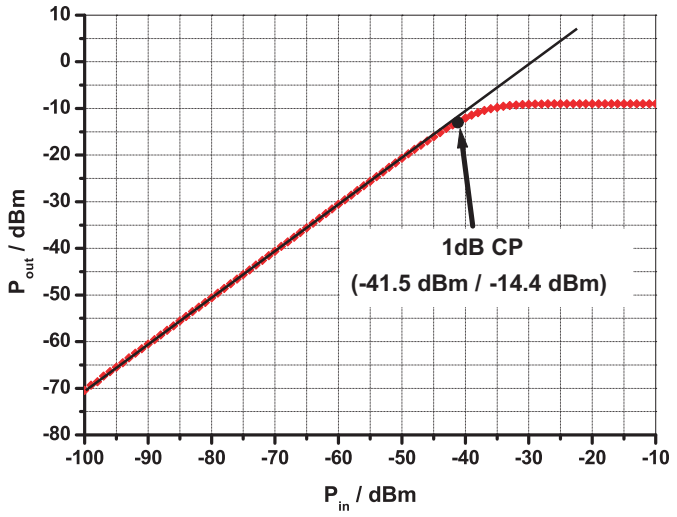

Fig. 7. Measured power transfer characteristic of the front-end at 22.5 GHz.

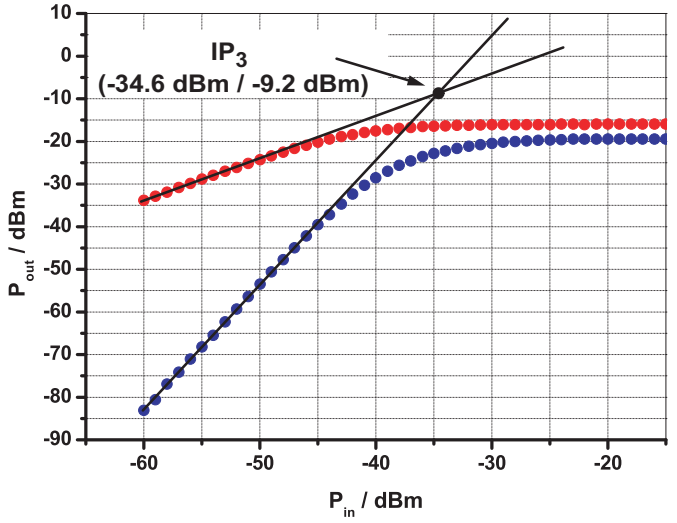

Fig. 8. Measured front-end two tone test, LO 17.7 GHz (3 dBm), RF 22.5 GHz \ 22.501 GHz.

Conclusions

An integrated 0.13 μm CMOS receiver front-end, for automotive and industrial sensor applications, is presented. The front-end aims at a fully integrated dual-conversion quasi-homodyne receiver. The presented front-end at 22.5 GHz features a gain of 25.8 dB, a SSB noise figure of 6.8 dB, an input IP3 of -34.6 dBm and an input 1 dB compression point of -41.5 dBm at a power consumption of 112.5 mW from 1.5 V supply voltage.

Table II shows an overview of recently published integrated front-ends. The measurement results of the realized front-end in combination with the high digital processing prowess of CMOS technology, opens the door for CMOS to emerge as a cost effective, low power system-on-chip receiver solution beyond 20 GHz.

TABLE II
Overview of recently published front-ends.

	[8]	[9]	[2]	This work
Total Power consumption	64.5 mW	-	470 mW	112.5 mW
Power Gain	27.5 dB	27.5 dB	16.3 dB	25.8 dB
Noise Figure	7.7 dB	7.5 dB	-	6.8 dB (SSB)
Frequency	21.8 GHz	23 GHz	24 GHz	22.5 GHz
Technology	0.18 μm CMOS	70 GHz-f_T SiGe BiCMOS	1.2 μm SiGe HBT	0.13 μm CMOS

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