Signal Integrity Analysis of a 1.5 Gbit/s LVDS Video Link

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***Abstract* — Future applications in luxury class cars may require digital video transmission with data rates as high as 1.5 Gbit/s. The signal integrity of an LVDS Serializer/Deserializer video link was investigated in this work from the viewpoint of the car manufacturer. Physically consistent simulation models for the driver, receiver, connectors, and cables were developed which are valid up to 3 GHz. Simulated and measured eye diagrams are compared and evaluated to obtain the maximum cable length as a function of data rate. Finally, the effect of pre-emphasis on the maximum cable length for various data rates was investigated.**

I. Introduction

Premium cars will feature video equipment components such as camera-based driver assistant systems and high resolution displays. These applications require digital video transmission between electronic control units via an electrical physical layer at data rates of about 1.5 Gbit/s over distances up to 15 m. Due to the short rise times of high-speed digital signals, frequency components up to 3 GHz need to be considered in the design process of the physical layer. The transmitted digital signals can experience unintentional reflections, interference, crosstalk, attenuation, distortion, and mode conversion on their way from the bus driver to the receiver. In the worst case bit errors could lead to failures in the application. With accurate simulation models, the signals at the receiver can be predicted and signal integrity can be verified in advance.

In a previous work Brandl et al. [1] analyzed the signal integrity of an LVDS (Low Voltage Differential Signaling) Serializer/Deserializer (SerDes) video link with up to 420 Mbit/s per differential channel. In the study of Goldie [2] eye diagram measurements of 780 Mbit/s were presented for an LVDS Display Interface. Ahn et al. [3] performed full wave simulation and transient simulations of coupled microstrip transmission lines for LVDS applications.

This paper investigates a 1.5 Gbit/s LVDS SerDes video link. Physically consistent simulation models up to 3 GHz were developed in the frequency domain for the driver, receiver, connectors, and cables, resp. Using Inverse Fourier Transform, eye diagrams were calculated for cable lengths and data rates of interest. Measured and simulated eye diagrams were compared and evaluated using an eye mask. The maximum cable length as a function of data rate was determined for different pre-emphasis settings.

Sections II–IV cover the LVDS Serializer/Deserializer, the HSD connector, and the Quad cable, resp. The signal integrity analysis of the complete signal path is presented in section V.

II. LVDS Serializer/Deserializer

Modern automotive navigation, driver information and entertainment modules are more and more converting from analog video to the higher quality RGB digital video format which is the standard and native interface towards LCD displays. Such interfaces can be addressed with point-to-point SerDes topologies and concepts. The SerDes chip sets reduce the number of transfer wires and connector pins in comparison to transporting a wide parallel bus. In this work, the DS90UR241/124 SerDes chip set from National Semiconductor was used. It serializes and deserializes 24 bits from and to a parallel LVTTL/LVCMOS data bus onto a single differential pair (Fig. 1). The chip set time multiplexes the parallel data and embeds the clock signals as a HIGH start bit and a LOW stop bit. This scheme also prevents any skew issues i.e. time delay between data and clock to occur over the transmission medium.

As longer cable connections may experience large ground potential shifts between transmitter and receiver module a so called AC coupling interfacing scheme is supported. The potentials of both transmitter and receiver modules are then decoupled by employing series capacitors in the transmission lines. A DC balance encoder in the serializer and a corre-

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sponding DC balance decoder in the deserializer provide an even dispersion between HIGH and LOW bits over the serial link. This means prevents any DC level biasing which may result in inter-symbol interference effects. With capacitors being employed on both sides this scheme also grants short circuit protection of the inputs/outputs in case a cable may break or exhibit short circuits to ground or vehicle power. The deserializer requires a $100\,\Omega$–termination resistor across its input pins while integrating bias circuitry that sets the operating point around an optimal common mode offset voltage of $1.2\,\mathrm{V}$.

For long cable runs, low pass filter effects of the cable, inter-symbol interference, phase noise, and skew can severely deteriorate the signal quality leading to increased bit error rate or even connection breakdown. By simulating and actually measuring eye diagrams at the receiver input and evaluating their opening versus the data sheet parameters potential problems of insufficient system margin can be identified during module development. Important parameters to crosscheck include the signal swing which should exceed receiver threshold region with margin or the transition point's phase noise/jitter which mustn't exceed the receiver's jitter tolerance. In case that voltage or timing margins need to be improved an optional signal conditioning by means of pre-emphasis (boost of drive current/signal amplitude during transition times) can be activated in the serializer output stage. The amount of signal boost is controlled by a resistor value tied to the pre-emphasis control pin.

The PLL frequency range of parallel data input/output clock supports LCD resolutions from Quarter-VGA (320x240) up to Wide-VGA (800x480) and beyond. The serial channel employs the EMC robust and low power LVDS electrical physical layer on the I/O level, standardized as ANSI-/TIA-/EIA-644A [4], [5].

Currently, there is no simulation model available that describes the considered SerDes chip set including pre-emphasis. Instead, three pulse sources connected in series

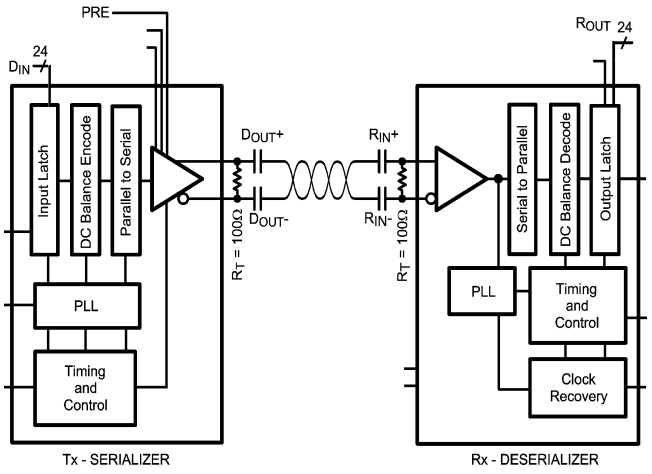

Fig. 1. LVDS Serializer/Deserializer concept.

were used to model the serializer's LVDS output. One source models the correct rise/fall times, voltage swing, and bit length. Depending on the bit pattern additional two sources are in or off phase to turn the 1-bit pre-emphasis on or off. Parasitic effects of the SerDes chip sets, AC capacitors and termination resistors were described with lumped equivalent circuit elements.

III. HSD Connector

Many concepts for differential signaling are based on either shielded or unshielded wire pairs that are twisted or untwisted. Low crosstalk between adjacent differential pairs is assured by shielding the pairs independently or by twisting the wires of each pair.

The HSD-concept follows a different approach: The four wires of the two differential lines are arranged in a twisted quad configuration as depicted in Fig. 2. Looking on one of

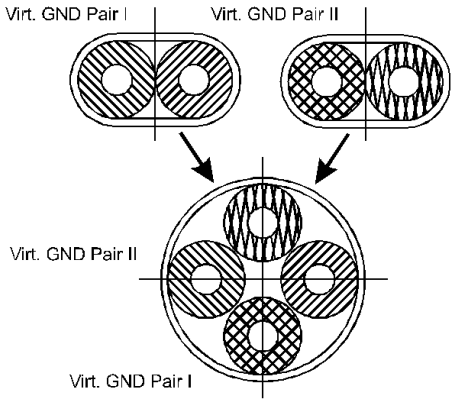

Fig. 2. Schematic drawing to illustrate the HSD-concept.

the pairs, the wires of the adjacent pair are located in the first pair's virtual ground plane. Crosstalk is therefore minimal. Measurements also show that this concept exhibits very low crosstalk-levels even though both differential pairs are covered by a common braid.

Similar to a coaxial interconnect, the outer conductor of the HSD-system provides an EMI-tight shielding to the signal path even at the interconnection plane as may be seen in Fig. 3. As a consequence the differential impedance of the connector is controlled and matched to the differential cable impedance. Also, EMI-emissions are extremely low. Emission levels of stripline measurements according to CISPR 25 of a data transmission at $800\,\mathrm{Mbit/s}$ were less than 12 dBµV up to 1 GHz.

Signal integrity measurements of the eye height vs. data rate using a bit error rate equipment in addition to electromagnetic full wave simulations clearly indicate that the main limitation of the bit rate is due to the impact of the cable. If the cable is sufficiently short, data rates of beyond $5\,\mathrm{Gbit/s}$ may be transmitted per differential pair.

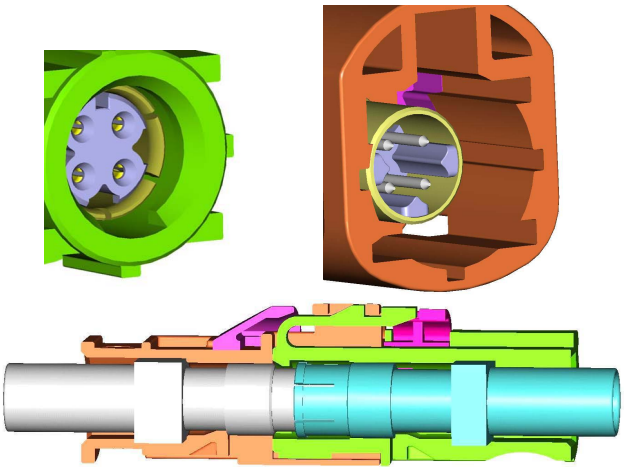

Fig. 3. 3D-view of the female (top left) and male HSD-interface (top right); cross-sectional view of a mated HSD-interconnect (bottom).

IV. Quad Cable

The Quad cable is proposed for high data rate signal transmission due to the outstanding RF properties and variety of application possibilities [6]. In this work a Quad cable consisting of four tin plated, stranded copper wires insulated with polypropylene was used. All four insulated wires are stranded with each other. An overall braided shield combined with a foil screen surrounds all wires and the screen is covered by a lead free PVC sheath (Fig. 4) [7]. The four signal wires

Fig. 4. Cross-sectional view (left picture) and side view (right picture) of a Quad cable.

can be used for either two differential transmission channels or one differential transmission channel plus power supply. In the Quad configuration, the near-end crosstalk (NEXT) of one differential pair to the other is below $-22\,\mathrm{dB}$ (Fig. 5). In addition, the differential to common mode conversion of one pair is less than $-25\,\mathrm{dB}$ which allows the differential mode to be described independently of the common mode. In the following sections, TEM propagation is assumed.

In conventional analytical transmission-line models, dielectric losses are treated as constant across all frequencies which leads to non-causal results [8]. Djordjevic et al. [9] presented a physically consistent model based on the Debey model, which was successfully applied by Hall et al. [10] to short transmission lines on FR4-PCBs. Their model considered a change in the transmission line impedance corresponding to a specific change in loss and the amount of energy propagated along the transmission line is a function of the energy dissipated.

In this work the basic model of Djordjevic has been adopted and applied to differential transmission on the more complex Quad cable. The model is based on the standard equivalent circuit transmission-line model with the frequency dependent per unit length elements: series $R'(\omega)$, series $L'(\omega)$, shunt $G'(\omega)$, and shunt $C'(\omega)$ which are defined as

$$R'(\omega) = \sqrt{(R'_{DC})^2 + (R'_{AC})^2}, \tag{1}$$

$$R'_{AC} = (1+\mathrm{j})\,\frac{R'_s(\omega_r)}{\sqrt{\omega_r}} \cdot \sqrt{\omega}, \tag{2}$$

$$L' = L'_o \tag{3}$$

R'_{DC} represents the ohmic conductor loss for the direct current component and $\mathrm{Re}\{R'_{AC}\}$ describes the skin effect loss and the proximity effect. ω is the angular frequency and ω_r is a constant reference angular frequency. Our measurements as well as simulation results in [8] show that $\sqrt{(R'_{DC})^2 + (R'_{AC})^2}$ describes the losses in the transition region between DC and the fully developed skin effect region more precisely than the expression $R'_{DC} + R'_{AC}$. The overall inductance consists of a frequency-independent outer inductance L'_o caused by currents flowing on the surface of the conductor and the inner inductance $\mathrm{Im}\{R'_{AC}\}/\omega$ which is caused by currents flowing inside the conductor.

The effective dielectric constant is modeled as

$$\varepsilon_{\mathrm{r,eff}}(\omega) = \varepsilon'_\infty + \frac{1}{\ln 10} \cdot \frac{\Delta\varepsilon'}{m_2 - m_1} \cdot \ln \frac{\omega_2 + \mathrm{j}\omega}{\omega_1 + \mathrm{j}\omega} \tag{4}$$

where $\Delta\varepsilon'$ represents the total variation between the lower frequency limit of the model $\omega_1 = 10^{m_1}\,\mathrm{s}^{-1}$ and the higher frequency limit $\omega_2 = 10^{m_2}\,\mathrm{s}^{-1}$ (here $m_1 = 0$ and $m_2 = 14$). $\Delta\varepsilon'/(m_2 - m_1)$ is the slope of the dielectric constant per decade and ε'_∞ the dielectric constant at very high frequencies. According to [11] and with $\varepsilon_{\mathrm{r,eff}}(\omega) = \varepsilon'(\omega) - \mathrm{j}\varepsilon''(\omega)$

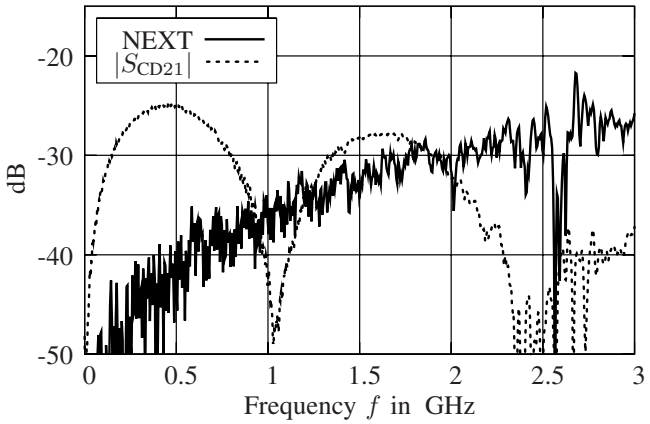

Fig. 5. Measured near-end crosstalk (NEXT) between two differential pairs and measured differential to common mode conversion of one differential pair for a cable length of 7.2 m.

Model Parameter	Value
R'_{DC} in mΩ/m	322
$R'_s(\omega_r)/\sqrt{\omega_r}$ in $\Omega\sqrt{s}$/m	$247.0 \cdot 10^{-6}$
L'_o in nH/m	486.7
$\Delta\varepsilon'$	0.094
ε'_∞	2.144
C'_0 in pF/m	22.06

TABLE I
EXTRACTED MODEL PARAMETERS.

we obtain

$$C'(\omega) = \varepsilon'(\omega) \cdot C'_0, \tag{5}$$

$$G'(\omega) = \frac{\varepsilon''(\omega)}{\varepsilon'(\omega)} \omega C'(\omega). \tag{6}$$

The frequency-independent model parameters were determined by fitting simulated S-parameters to measured S-parameters using a gradient optimizer; the optimized model parameters are listed in Table I. They are physically reasonable since they are close to values calculated with approximations. Note that the complex-valued effective dielectric constant includes the dielectrics polypropylene and air.

The per-unit length elements make it possible to separate the ohmic and dielectric losses and allow them to be reduced by, for example, selecting different materials or changing conductor diameters.

The transmission-line model accurately describes the frequency response of phase velocity v_p and forward transmission coefficient $|S_{\mathrm{CD21}}|$ (Fig. 6). The phase velocity increases

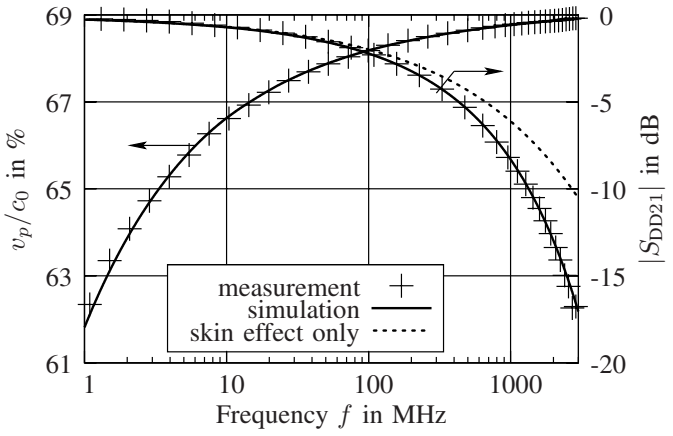

Fig. 6. Measured and simulated differential phase velocity and differential forward transmission coefficient for a cable length of 7.2 m.

with frequency mainly because of a decreasing inner inductance. Skin effect losses dominate dielectric losses and both cause a low-pass characteristic as can be seen in the forward transmission coefficient curve. Digital signals are distorted for faster propagation of higher-frequency components and are much stronger attenuated which as a consequent causes a degradation in rise time of digital signals.

The step response of the transmission line was measured with differential Time-Domain-Transmission (TDT) equipment (input step-rise time of 17 ps). It was also simulated and the simulated step response was found by using Inverse Fourier Transform to the frequency response of a step function (Fig. 7). The conventional model with constant dielectric

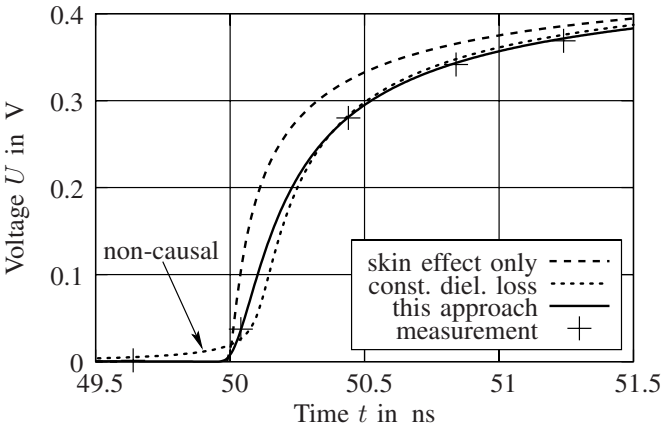

Fig. 7. Measured and simulated differential step response for a cable length of 7.20 m. The model with frequency independent dielectric losses produces non-causal behavior. In contrast, the approach in this work is causal.

losses produces non-causal behavior. By contrast, the model developed above is causal. The measured step response agrees well with the simulated data and the rise-time degradation due to ohmic and dielectric losses is considerable.

V. SYSTEM SIGNAL INTEGRITY

The complete differential signal path has to be considered when analyzing the quality of the digital signals at the receiver. In particular, the investigated signal path consists of:

1) LVDS serializer, termination, and coupling capacitors,
2) HSD connector,
3) Quad cable of variable length,
4) HSD connector,
5) Coupling capacitors, termination, and deserializer.

The results above show increasing attenuation of the cable by increasing cable length and frequency. Information about the maximum cable length as a function of data rate can be measured or predicted from system simulations.

The models developed above are combined to an overall model of the differential signal path and can be included in a harmonic balance simulation (ADS was used). Using Inverse Fourier Transform, time domain results are obtained and eye diagrams can be generated. The alternative in using transient simulation in combination with a convolution simu-

lator that allows incorporating frequency-domain models was less accurate. A pseudo-random bit sequence of 1024 bit was used to generate the eye diagrams in the simulation. In the following eye diagrams the differential voltage V_{D} at either the transmitter or the receiver is plotted against time.

Fig. 8(a) , 8(b) show a measured and simulated eye diagram (770 Mbit/s at 10 m) with the specified dashed eye mask. At the receiver the signal rise time is degraded which causes inter-symbol interference with jitter. In this case the simulated eye complies with the eye mask and the data transmission is ensured.

Pre-emphasis is a cost effective fixed-equalization method to partially pre-compensate the signal distortion caused by the cable. At each binary signal transition the signal edge with its high frequency components is transmitted with an overshoot of adjustable size; in this work pre-emphasis was set to twice the regular voltage swing.

The effect of pre-emphasis is illustrated in Fig. 8(c)–8(f). As discussed above the attenuation and the jitter for 10 m cable length at 770 Mbit/s without pre-emphasis is significant. In the case of transmission with pre-emphasis, the eye height and eye width are enlarged. Measured and simulated eye diagrams agree well.

Eye diagram simulations for the data rates 0.84 Gbit/s, 1.20 Gbit/s, 1.54 Gbit/s, and 2.02 Gbit/s, resp. were performed for cable lengths in steps of 1 m with and without pre-emphasis. They are compared to measurements for the available cable lengths of 5 m, 7 m, 10 m, and 13 m, resp. The maximum cable length across data rate is plotted in Fig. 9.

As expected the maximum cable length decreases with an increasing data rate. The maximum cable length without pre-emphasis can be extended to more than 50% by using pre-emphasis and measured and simulated data agree well with each other.

VI. Conclusion

The signal integrity of a 1.5 Gbit/s LVDS video link was investigated in this paper. Physically consistent simulation models have been developed for the Serializer/Deserializer, HSD connector, and Quad cable. The complete signal path was investigated based on these models and simulated eye diagrams agree well with measurements. The maximum cable length as a function of data rate is determined by simulations and verified by measurements. Using pre-emphasis allows to extend the maximum cable length to more than 50%.

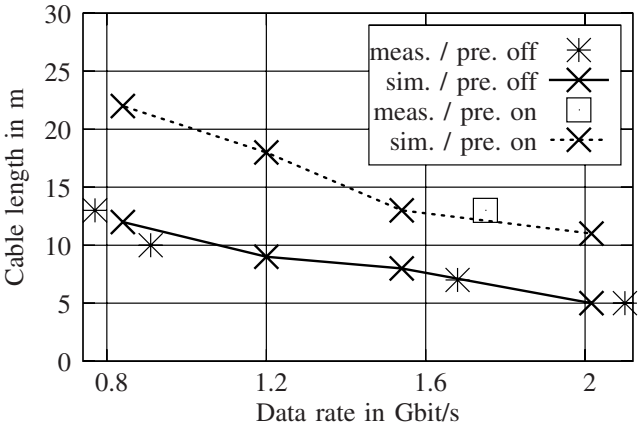

Fig. 9. Measured and simulated maximum cable length as a function of data rate with and without pre-emphasis.

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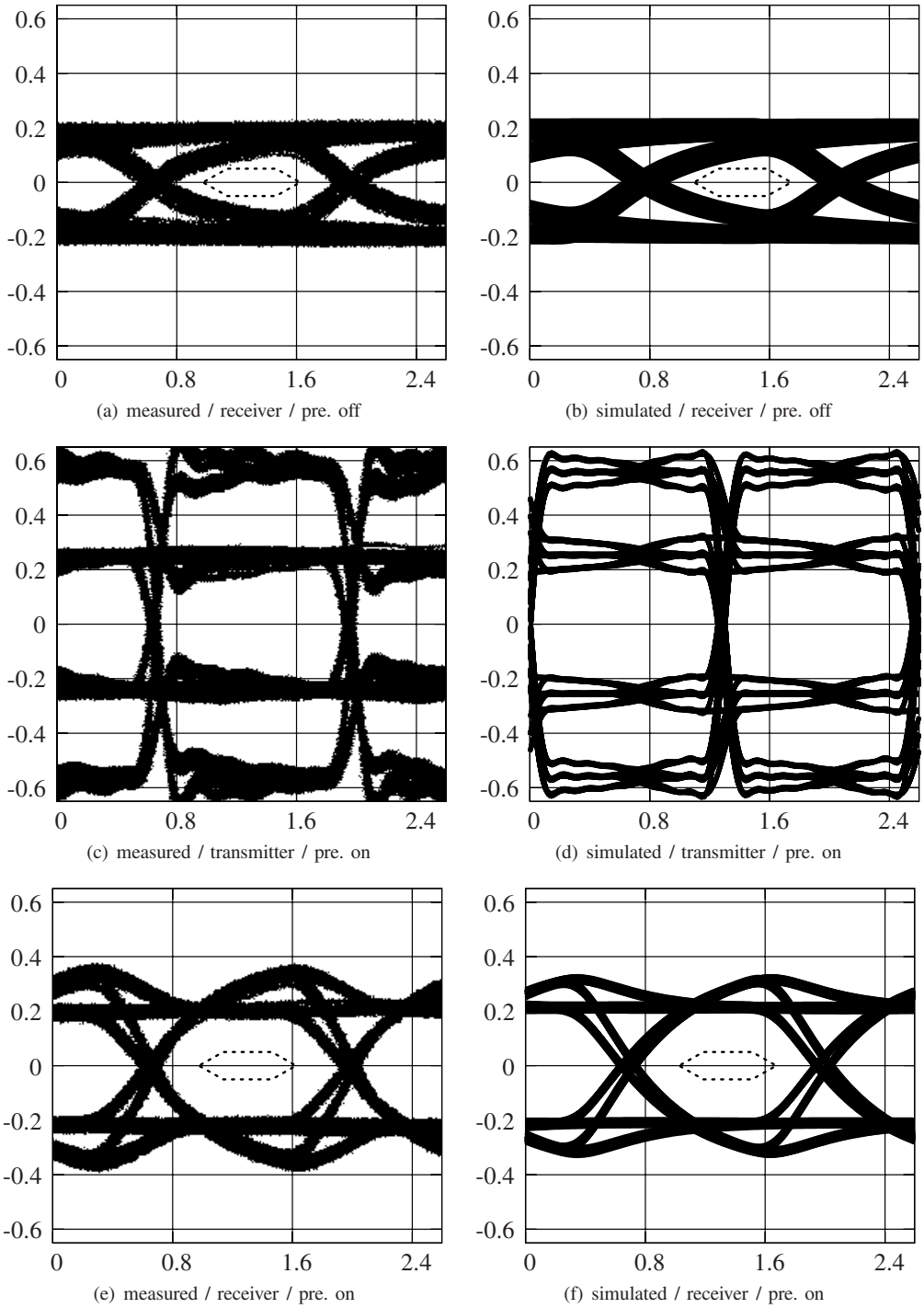

(a) measured / receiver / pre. off

(b) simulated / receiver / pre. off

(c) measured / transmitter / pre. on

(d) simulated / transmitter / pre. on

(e) measured / receiver / pre. on

(f) simulated / receiver / pre. on

Fig. 8. Measured (left column) and simulated (right column) eye diagrams. In all diagrams the differential voltage V_{D} in V is plotted vs. time in ns for the data rate of 770 MBit/s over a cable length of 10 m.